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Simulation of Novel 15-Level Cascaded Inverters Using Proposed RSPWM Technique for Connecting to the Grid

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***Abstract*— Inverter is one of the most important parts in a grid-connected single-phase photovoltaic system. In this paper, two new cascaded inverters which are used for the grid-connected systems have been introduced and simulated. These proposed inverters are two new inverters, which each one has two cascaded full-bridges inverter. These structures, because of the different input voltage in each of the full-bridges, are called asymmetric cascaded inverters. In these Inverters, the changes have been created in one of the full-bridges that lead to the difference between two full-bridges from each other. Changing in one of the full-bridges and the feature of the asymmetry are leading to increase the number of voltage levels at the inverter output. Also, for controlling the proposed Inverters, reverse sinusoidal pulse width modulation (RSPWM) technique is used. Finally, in these two proposed topologies, the quality of output voltage waveform is improved, and voltage harmonics and total harmonic distortion (THD) are reduced. In this article, some features of these two new converters and comparison of them with each other are given. PSCAD software is used for simulation of these converters**.

Keywords- Multilevel inverters, Cascaded full bridge inverter, Output voltage quality, Total harmonic distortion (THD)

1. Introduction

The increasing energy consumption, costs of the fossil fuels and being non-renewable have caused a fast and big development in renewable systems. One of these power generation systems is photovoltaic (PV) systems. The produced energy from PV systems can be delivered to the power grid system by connecting inverter to the grid. An inverter connected to single phase grid is usually applied for household or low power application, which the power range is less than 10Kw [1]. A lot of types of inverters that connected to single phase grid has examined in several literature [2]. Full bridge three-level inverter topology is more popular than others, but three-level inverters due to their more switching numbers, increase the acoustic noise, switching losses, and electromagnetic interference (EMI). Voltage harmonics, the size of used filter and generated EMI are reduced by increasing the number of output voltage levels [3]. The new multilevel topologies have approximately sinusoidal output voltage waveforms and output current with less distortion [3] and [4].

In recent years, different topologies of the multilevel inverters have suggested. The most common topology are diode clamped inverter [5], inverters having floating capacitor [6], inverters with cascaded H bridges [7] and [8], and multilevel inverters having improved H bridge [9]. In some new topologies, transformer is eliminated from the PV converter structure. In fact, passive elements that applied in output filter are employed for eliminating harmonics, and they are actually the massive components of circuit. Therefore, by decreasing the size of filter, it is possible to reduce the weight and cost and consequently increasing the efficiency. Multilevel converters have been studied for many years, and perform much better than two-level and three-level popular converters [10]. The proposed topology in [11] includes two asymmetric cascaded full bridges. In this topology, two different DC voltage sources supply the voltage for each full bridge. By a proper control of the ratio between two voltages, various sets of output levels can be obtained. If the voltage of the layer with lower DC voltage equal to $\frac{1}{3}$ of the voltage of the layer with higher DC voltage, nine levels of output voltage will be generated. Two extra low power switches, and a switching service including a switch and a diode bridge are adopted in final topology in order to reduce the ground leakage current. The proposed inverter in [12] has been used in a PV system connected to grid, in which a boost DC-DC converter is included in order to enhance the output voltage of inverter V_{in} such that it is more than $\sqrt{2}$ times of grid voltage V_{grid} to guarantee the power flow of PV arrays into grid.

In this paper, a cascaded inverter consisted of two full bridges is introduced and simulated in second part. In third part, by developing the changes in one of the bridges of available cascaded inverter, two new inverters are proposed. In fourth part, the simulation results of the inverters are shown. Finally the conclusions of this paper are presented in fifth part.

2. Cascaded inverter with two full bridges

2.1. Nine-level cascaded inverter

The proposed inverter in [13] includes two full bridges, which are connected together in cascaded form. That is why, it is named two-layer inverter. The topology of this inverter is illustrated in Figure 1, which one of the bridges (the layer with voltage V_{dc1}) has a power supply voltage V_{dc1}=300v, and the other bridge voltage is considered as V_{dc2}. Thus, the voltages of these layer are different, if $V_{dc2} = \frac{1}{3}V_{dc1}$, the inverter will finally generate nine levels of voltage, and it is named a nine-level asymmetric cascaded inverter. If $V_{dc2} = \frac{1}{2}V_{dc1}$, the inverter will finally generate seven levels of voltage, and it have more output voltage than the previous mode. If the voltage of two layers be equal, the inverter possesses five levels of voltage, and for this case, inverter is named a symmetrical inverter with having more output voltage than two previous modes.

The cascaded inverters topology with two asymmetric bridges is shown in Figure 1, where $V_{dc2} = \frac{1}{3}V_{dc1}$, actually, power supply voltage of this layer is considered equal to 100v. Output voltage of these layers is considered as low voltage (LV) and high voltage (HV), and the total voltage of these two layers is expressed with V_{in}, and the number of output levels are determined here.

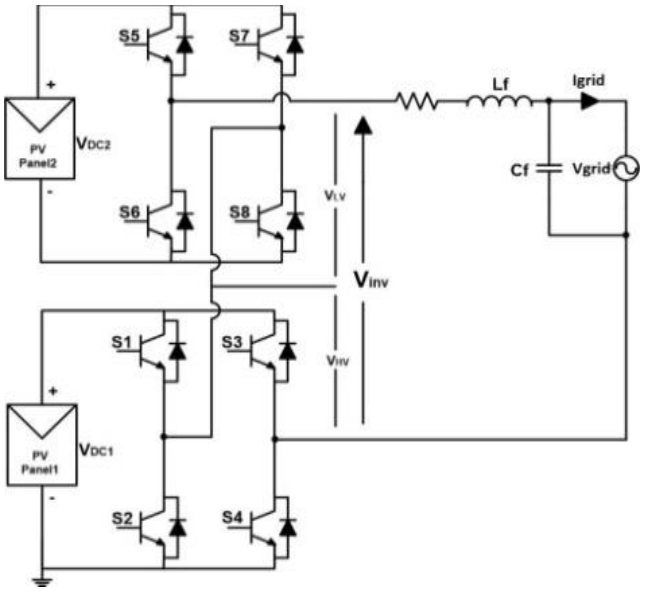


Figure 1. Cascaded inverter topology with two asymmetric layers

2.2. Revers sinusoidal pulse width modulation technique

For control of this inverter, a new revers sinusoidal pulse width modulation (RSPWM) control technique is adopted to produce switching signals related to switches of this inverter [9]. In RSPWM technique, where the base sinusoidal signal is larger than the triangular signal, pulses with magnitude of one are produced, and where the base signal is less than the triangular signal, zero pulses are produced. To generate a voltage with nine levels in output, four equal sinusoidal reference or base signals should be compared with a triangular carrier signal. So that each reference signal has a displacement value relative to the other, and this displacement (distance) is equal to the size of the carrier wave signal. In addition, the carrier signal frequency must be multiple of the reference signal frequency. In Table 1, levels of the output voltage, turned on and off switches according to each level of voltage are defined.

Table 1. Produced levels of the nine-level inverter and turned on and off switch in each level

level	V_{inv}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
L_1	$V_{dc1}+V_{dc2}$	on	off	off	on	on	off	off	on
L_2	V_{dc1}	on	off	off	on	off	on	off	on
L_3	$V_{dc1}-V_{dc2}$	on	off	off	on	off	on	on	off
L_4	V_{dc2}	off	on	off	on	on	off	off	on
L_5	0	off	on	off	on	off	on	off	on
L_6	$-V_{dc2}$	off	on	off	on	off	on	on	off
L_7	$-V_{dc1}+V_{dc2}$	off	on	on	off	off	off	off	off
L_8	$-V_{dc1}$	off	on	on	off	off	on	off	on
L_9	$-V_{dc1}-V_{dc2}$	off	on	on	off	off	on	on	off

Figure 2 illustrates the produced switching signals by RSPWM technique in one period for the carrier signal frequency, which is 20 times of the reference signal frequency, where the reference signal frequency is considered equal to 60Hz. For zero voltage level, two switching modes are happened, but in order to reduce the number of switching and losses, just one mode for zero voltage level is considered.

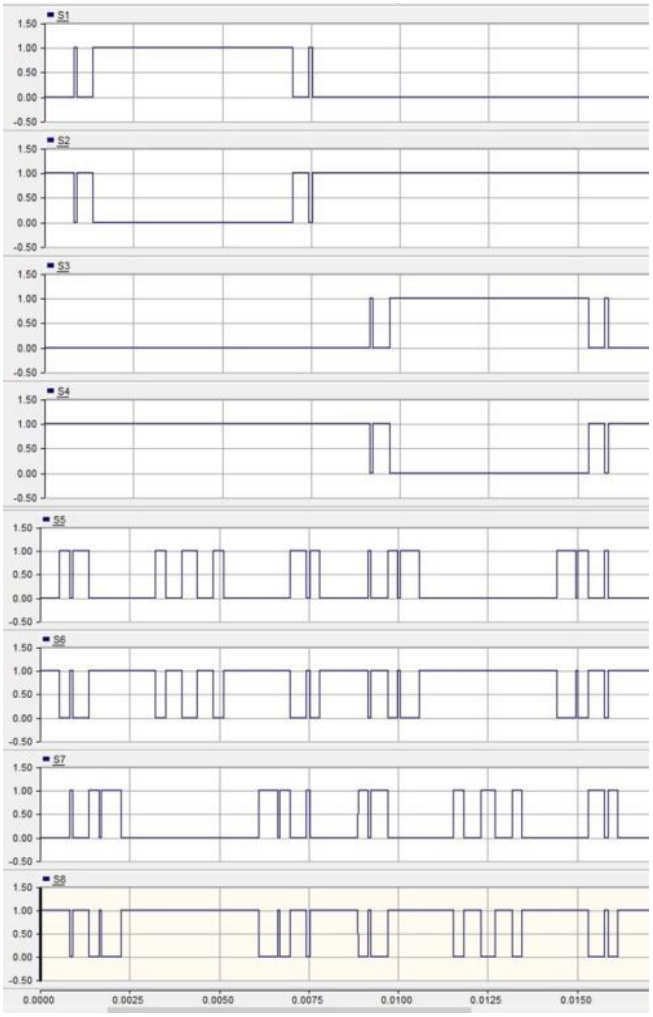
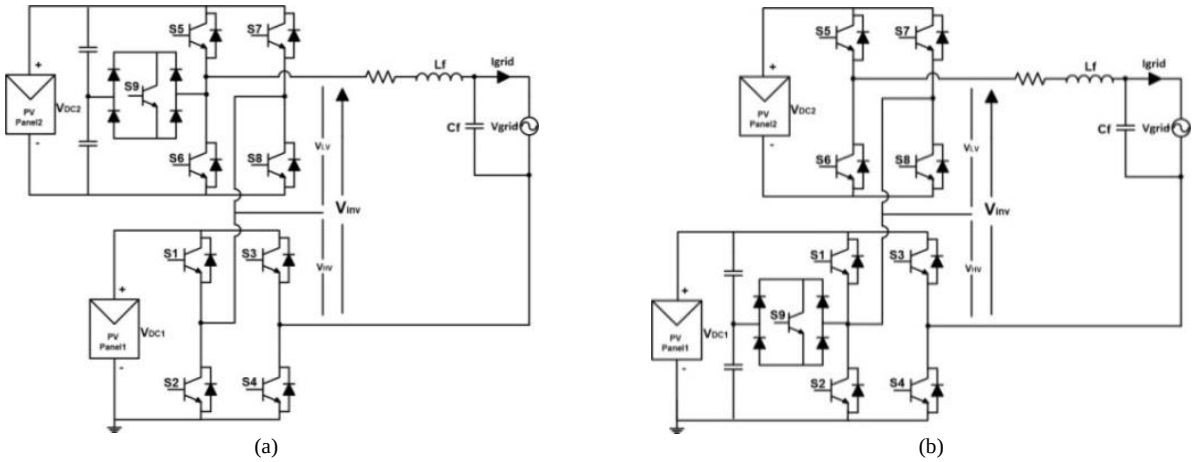


Figure 2. Produced switching signals by RSPWM technique in one period

3. The topology of the proposed cascaded inverter

In this section, two different cascaded inverters are proposed. While both of them contain two asymmetric full bridges, a special different algorithm is used for switching each inverter. The topologies of corresponding to these two inverters are represented in Figure 3. Moreover, both inverters are connected to grid without any transformer. The difference in the appearance of these topologies is related to the auxiliary switch, that in Figure ۳a, the auxiliary switch is used in the low voltage layer, which causes half of V_{dc2} in this layer. In Figure 3b, the auxiliary switch is adopted in the high voltage layer to create the half of the voltage V_{dc1}. V_{dc1} is different in these two converters as well as and V_{dc2}. In both converters, the value of V_{dc2} is less than V_{dc1}. In the inverter of Figure3a, the voltage V_{dc2} has been considered equal to $\frac{2}{5}$ V_{dc1} and in the inverter of Figure3b, the voltage V_{dc2} has been considered equal to $\frac{1}{5}$ V_{dc1} that generate 15-level voltage in inverter output.



(a) (b)

Figure 3. (a) Inverter with auxiliary switch in low voltage layer; (b) Inverter with auxiliary switch in high voltage layer

In both inverters, the switches S_1 to S_8 are related to two full bridges, and S_9 is the mentioned auxiliary switch. The main advantage of the auxiliary switch is that it causes the number of levels of a full bridge to be increased from three levels to five levels. Thus, these two layers finally develop 15 levels of voltage in the output of the cascaded inverter.

In the proposed inverters, $V_{dc1} + V_{dc2} = 400v$. Although V_{dc1} and V_{dc2} of the inverter of Figure 3a are different from V_{dc1} and V_{dc2} of the inverter of Figure 3b, levels of output voltage for both of these two inverters are exactly equal. The generated levels from the inverter of Figure 3a are as follow:

The layer with auxiliary switch shown in (1):

$$-V_{dc2},\quad -V_{dc2}/2,\quad 0,\quad V_{dc2}/2,\quad V_{dc2} \tag{1}$$

The layer without the auxiliary shown in (2):

$$-V_{dc1},\quad 0,\quad V_{dc1} \tag{2}$$

where V_{dc1} and V_{dc2} are as follows:

$$V_{dc1} = \frac{5}{7}(V_{dc1} + V_{dc2}) = \frac{5}{7}400v = 285.7143v \tag{3}$$

$$V_{dc2} = \frac{2}{7}(V_{dc1} + V_{dc2}) = \frac{2}{7}400v = 114.2857v \tag{4}$$

The generated levels of output voltage from the inverter of Figure ۳b are as follow:

The layer with auxiliary switch shown in (5):

$$-V_{dc1},\quad -V_{dc1}/2,\quad 0,\quad V_{dc1}/2,\quad V_{dc1} \tag{5}$$

The layer without the auxiliary shown in (6):

$$-V_{dc2},\quad 0,\quad V_{dc2} \tag{6}$$

where V_{dc1} and V_{dc2} are as follows:

$$V_{dc1} = \frac{6}{7}(V_{dc1} + V_{dc2}) = \frac{6}{7}400v = 342.8571v \tag{7}$$

$$V_{dc2} = \frac{1}{7}(V_{dc1} + V_{dc2}) = \frac{1}{7}400v = 57.1429v \tag{8}$$

In RSPWM technique for both of these two inverters, because of generating 15 levels of voltage in output, seven reference sinusoidal signals with a frequency 60Hz and a triangular carrier signal with a multiple times of the frequency 60Hz must be employed to produce RSPWM switching signals for all switches of inverters, which is illustrated in Figure 4. It is necessary to mention the displacement between reference signals is equal to peak to peak of carrier signal. In Figure 4, carrier signal frequency is considered 20 times of reference signal frequency.

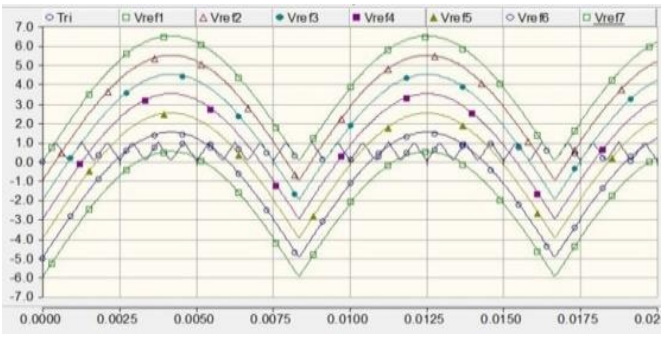


Figure 4. Comparing 7 sinusoidal reference signals and a triangular carrier signal in RSPWM technique for 15-level inverters.

4. Simulation results

These inverters are simulated by PSCAD/EMTDC software. In all simulations, the grid voltage is considered as 220v, the reference frequency is 60Hz and the carrier signal frequency (switching frequency) is 9kHz. Because of the difference in the location of auxiliary switch in two proposed inverters, the produced switching signals for these two inverters are also different, but due to equal number of levels, ultimately, both converters produce 15 levels of voltages. Compared with a nine-level inverter, the number of levels has increased, and waveform has approached to sinusoidal waveform. Figure 5a shows nine-level voltage of cascaded inverter without auxiliary switch, and Figure 5b shows the grid current of nine-level inverter.

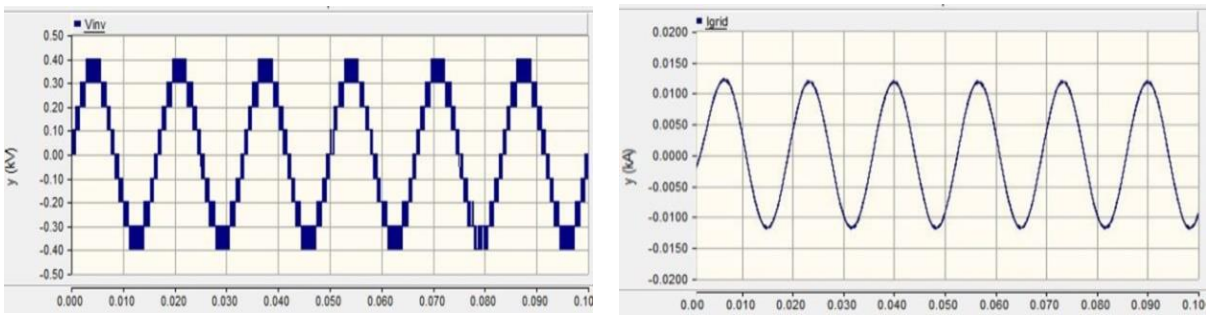
Table 2 shows how to turn switches of the inverter of Figure 3a on and off at each voltage level, Table 3 shows how to turn switches of the inverter of Figure 3b on and off at each voltage level. It can be seen switching algorithms of these two converters are different, but output voltages of them are approximately similar. In Figure 6, output voltages of these two inverters are shown, As the number of output voltage levels in inverters with auxiliary switch have increased, therefore output voltage waveform is closer to sinusoidal wave. The grid voltage $(220\sqrt{2}v)$ for these three inverters is shown in Figure 7.

Table 2. The generated levels by inverter and turned on and off switches in each level of inverter figure 3a.

level	V_{inv}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
L_1	$V_{dc1}+V_{dc2}$	on	off	off	on	on	off	off	on	off
L_2	$V_{dc1}+V_{dc2}/2$	on	off	off	on	off	off	off	on	on
L_3	V_{dc1}	on	off	off	on	off	on	off	on	off
L_4	$V_{dc1}-V_{dc2}/2$	on	off	off	on	off	off	on	off	on
L_5	$V_{dc1}-V_{dc2}$	on	off	off	on	off	on	on	off	off
L_6	V_{dc2}	off	on	off	on	on	off	off	on	off
L_7	$V_{dc2}/2$	off	on	off	on	off	off	off	on	on
L_8	0	off	on	off	on	off	on	off	on	off
L_9	$-V_{dc2}/2$	off	on	off	on	off	off	on	off	on
L_{10}	$-V_{dc2}$	off	on	off	on	off	on	on	off	off
L_{11}	$-V_{dc1}+V_{dc2}$	off	on	on	off	on	off	off	on	off
L_{12}	$-V_{dc1}+V_{dc2}/2$	off	on	on	off	off	off	off	on	on
L_{13}	$-V_{dc1}$	off	on	on	off	off	on	off	on	off
L_{14}	$-V_{dc1}-V_{dc2}/2$	off	on	on	off	off	off	on	off	on
L_{15}	$-V_{dc1}-V_{dc2}$	off	on	on	off	off	on	on	off	off

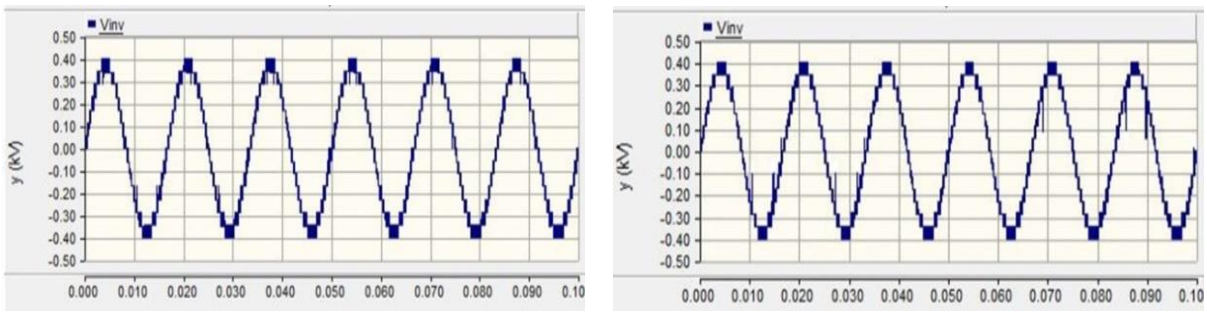
Table 3. The generated levels by inverter and turned on and off switches in each level of inverter figure 3b.

level	V_{inv}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
L_1	$V_{dc1}+V_{dc2}$	on	off	off	on	on	off	off	on	off
L_2	V_{dc1}	on	off	off	on	off	on	off	on	off
L_3	$V_{dc1}-V_{dc2}$	on	off	off	on	off	on	on	off	off
L_4	$V_{dc1}/2+V_{dc2}$	off	off	off	on	off	off	off	off	on
L_5	$V_{dc1}/2$	off	off	off	on	off	on	off	on	on
L_6	$V_{dc1}/2-V_{dc2}$	off	off	off	on	off	on	on	off	on
L_7	V_{dc2}	off	on	off	on	off	off	off	off	off
L_8	0	off	on	off	on	off	on	off	on	off
L_9	$-V_{dc2}$	off	on	off	on	off	on	on	off	off
L_{10}	$-V_{dc1}/2+V_{dc2}$	off	off	on	off	off	off	off	off	on
L_{11}	$-V_{dc1}/2$	off	off	on	off	off	on	off	on	on
L_{12}	$-V_{dc1}/2-V_{dc2}$	off	off	on	off	off	on	on	off	on
L_{13}	$-V_{dc1}+V_{dc2}$	off	on	on	off	off	off	off	off	off
L_{14}	$-V_{dc1}$	off	on	on	off	off	on	off	on	off
L_{15}	$-V_{dc1}-V_{dc2}$	off	on	on	off	off	on	on	off	off



(a) (b)

Figure 5. (a) Output voltage of nine-level inverter; (b) Grid current



(a) (b)

Figure 6. (a) Output voltage of 15-level inverter topology of Figure 3a; (b) Output voltage of 15-level inverter topology of Figure 3b.

To explain the operation of these two proposed 15-level inverters, as an example, the level 4 for both inverters is analysed.

In the inverter of Figure 3a, the level 4 in Table 2 is $V_{dc1}-V_{dc2}/2$, according to half of input voltage generated in second layer, the auxiliary switch is used in second layer (low voltage). For this inverter, $V_{dc1}=285.7143v$, and $V_{dc2}=114.2857v$. Concerning the equation of the level 4, the voltage in this level is given as:

$$V_{dc1}-V_{dc2}/2=285.7143-57.1429=228.5714v \quad (9)$$

In the inverter of Figure 3b, according to Table 3, the level 4 is $V_{dc1}/2+V_{dc2}$, according to half of input voltage generated in first layer, the auxiliary switch is used in first layer (high voltage). For this inverter, $V_{dc1}=$

342.8571v, and $V_{dc2} = 57.1429$v, and concerning the equation of the level 4, the voltage in this level is given as:

$$V_{dc1}/2 + V_{dc2} = 171.4285 + 57.1429 = 228.5714v \quad (10)$$

Concerning to the voltage which is obtained from level 4 in 15-level inverters, it is resulted that equations corresponding to each level in both inverters are different, but the voltage of this level in both of inverters are equal. The voltage of other levels can be given by Table 2 and Table 3. It can be shown that the voltages of other levels are equal too. Different location of auxiliary switch in these two inverters causes the equation of each level in the inverters to be different, and two inverters create the different total harmonic distortions, different voltage harmonics, different output powers, and different efficiencies.

The value of voltage harmonics (the total input voltage to each three inverters is 400v, which means $V_{dc1} + V_{dc2} = 400$v) of nine-level inverter and two proposed 15-level inverters up to harmonic of 63th-order have shown in Fig 8 and Figure 9.

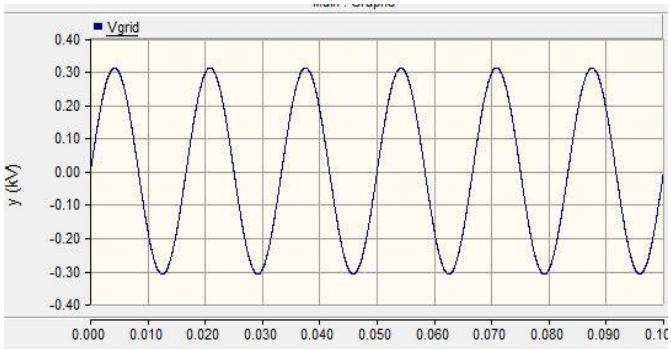


Figure 7. Grid voltage for three presented inverters

Figure 8 represents harmonics of output voltage of 9-level inverter, as can be seen, main harmonic value is 349.828v, which embraces 87.46 percent of harmonics. Figure 9a indicates output voltage harmonics of 15-level inverter related to Figure 3a, here, it can be seen that the value of main harmonic is 370.484v, which encompasses 92.62 percent of harmonics. Figure 9b demonstrates output voltage harmonics of 15-level inverter related to Figure 3b, as can be seen, the value of main harmonic is 370.453v, which includes 92.61 percent of harmonics. From the figures, it can be seen that the value of main harmonic of 15-level inverters is more than 9-level inverter, and main harmonic of 15-level inverter shown in Figure 3a is more than the inverter shown in Figure 3b. When the auxiliary switch is placed in the high voltage layer, losses increase, and output power also decreases.

By increasing the carrier frequency, the lower order harmonics will be reduced, in fact, harmonics move to higher orders, but switching losses increase, which results lower output power and efficiency.

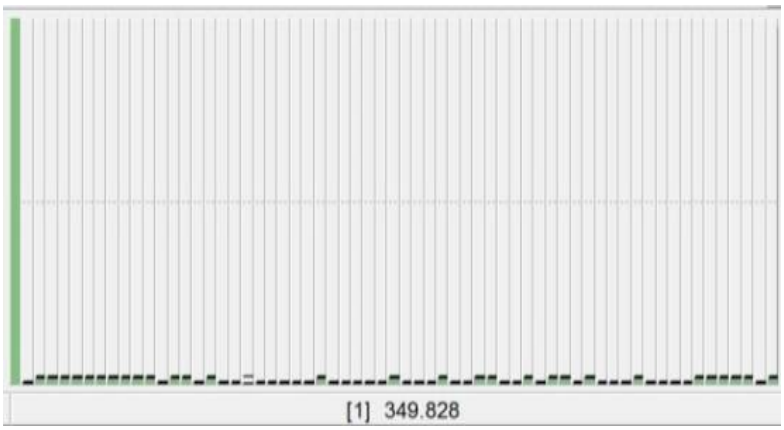
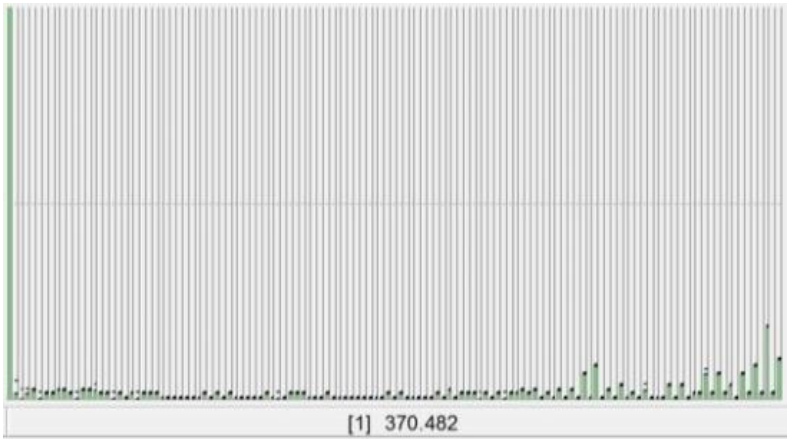
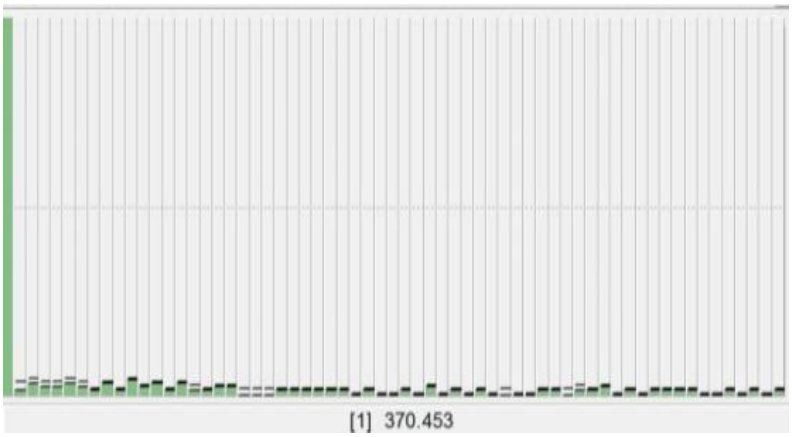


Figure 8. Value of voltage total harmonic distortion in nine-level inverter



(a)



(b)

Figure 9. Value of harmonics and voltage total harmonic distortion of two proposed 15-level inverters: (a) inverter Figure 3a; (b) inverter Figure 3b

Another issue which is shown in this paper and in these inverters is that the employed filter in output of nine-level inverter is greater than the employed filter in 15-level inverters [14]. In other words, 15-level inverter compared to nine-level inverter needs a smaller filter. The value of capacitor and inductor adopted in the filter of nine-level inverter are 25µf and 7mH respectively, and the value of capacitor and inductor adopted in the filter of both proposed 15-level inverters are 1µf and 5mH respectively.

In the desired photovoltaic system in this paper, by adopting the inverter described, the transformer which is an expensive and heavy component, has been deleted, that saves both economic costs and less space.

The reverse sinusoidal pulse width modulation technique (RSPWM), despite the advantages such as smaller filters, removing low order harmonics, has disadvantages such as increasing switching losses and begetting acoustic noise. Floating capacitor used in DC-link must contain suitable capacity, because high-capacity capacitors are not affordable, and low-capacity capacitors have adverse effects on the output waveform of inverter and the grid current.

5. Conclusion

RSPWM technique is used for all inverters to generate switching signals, which decreases voltage harmonics, and distortion according to approximately sinusoidal waveform in output of inverter. Having an auxiliary switch in the circuit of the proposed inverters in this paper, the numbers of levels from nine levels to 15 levels are increased. By developing more sinusoidal waveform, less harmonics, and less distortions of harmonic are obtained. Moreover, a smaller filter is employed in output of proposed inverters. Finally, it must be said that the inverter with auxiliary switch in low voltage layer compared to the inverter with auxiliary switch in high voltage layer has a less voltage distortion.

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