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Silicon Photonic Integrated Nano Cavity

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***Abstract*—Silicon photonic as the platform for the integrated optoelectronic and photonic circuits is the base of photonic devices and systems' design and constructions. In this article, a silicon photonic based nano cavity is introduced. The 3D – FDTD simulation results are presented. Silicon photonic circuits are well suited for dual-polarization optical coherent transmitters and receivers.**

Keywords-silicon photonic; integrated circuits; nano cavity

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1. Main text

Silicon photonics is the study and application of photonic systems which use silicon as an optical medium. The silicon is usually patterned with sub-micrometre precision, into microphotonic components. These operate in the infrared, most commonly at the 1.55 micrometre wavelength used by most fiber optic telecommunication systems. The silicon typically lies on top of a layer of silica in what (by analogy with a similar construction in microelectronics) is known as silicon on insulator (SOI) [1] to [3].

Silicon photonic devices can be made using existing semiconductor fabrication techniques, and because silicon is already used as the substrate for most integrated circuits, it is possible to create hybrid devices in which the optical and electronic components are integrated onto a single microchip [4] to [5].

In this work, a simple nano cavity made of silicon cylinder on the silicon photonic substrate is introduced. The FDTD theoretical simulation results demonstrate the optical field concentration within the designed structure.

1.1. Structure design and simulation

The designed integrated nano cavity made of silicon nano cylinder located on the silicon substrate is shown in Figure 1. The silicon nano cylinder has the radius of about 0.3 micrometer and the height of 40 nm.

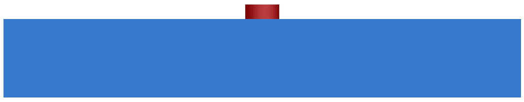

Figure 1. Side view of the integrated silicon photonic nano cavity

The designed integrated structure is excited by an x – polarized electric dipole as the incident optical source. The optical source is illuminated the structure from the substrate side. A perfectly matched layer (PML) is used as the boundary condition for 3D simulations. The PML is an artificial absorbing layer for wave equations, commonly used to truncate computational regions in numerical methods to simulate problems with open boundaries, especially in the FDTD and FE methods.

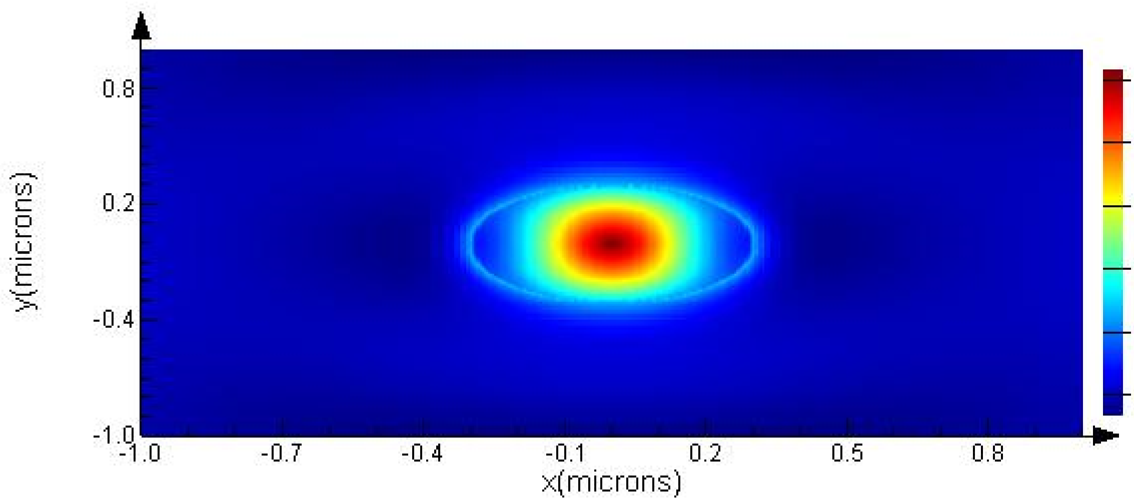

Figure 2. Electrical field in the interface between silicon substrate and silicon cylinder

The 3D simulation results that is the result of monitoring the optical electrical field confined in the interface between the silicon cylinder and the silicon substrate is demonstrated in Figure 2.

As shown in this Figure the optical field is concentrated in the interface is improved by about 1.12 times respect to the input field.

Repeating the simulation by monitoring the optical field in the middle of the nano cylinder, we achieve the optical electric filed shown in figure 3. The incident optical field is improved by more than 5 times in the centre of nano cylinder.

Magnetic field achieved in the hybrid structure is shown in figure 4. The magnetic field has been monitored in the centre of silicon nano cylinder.

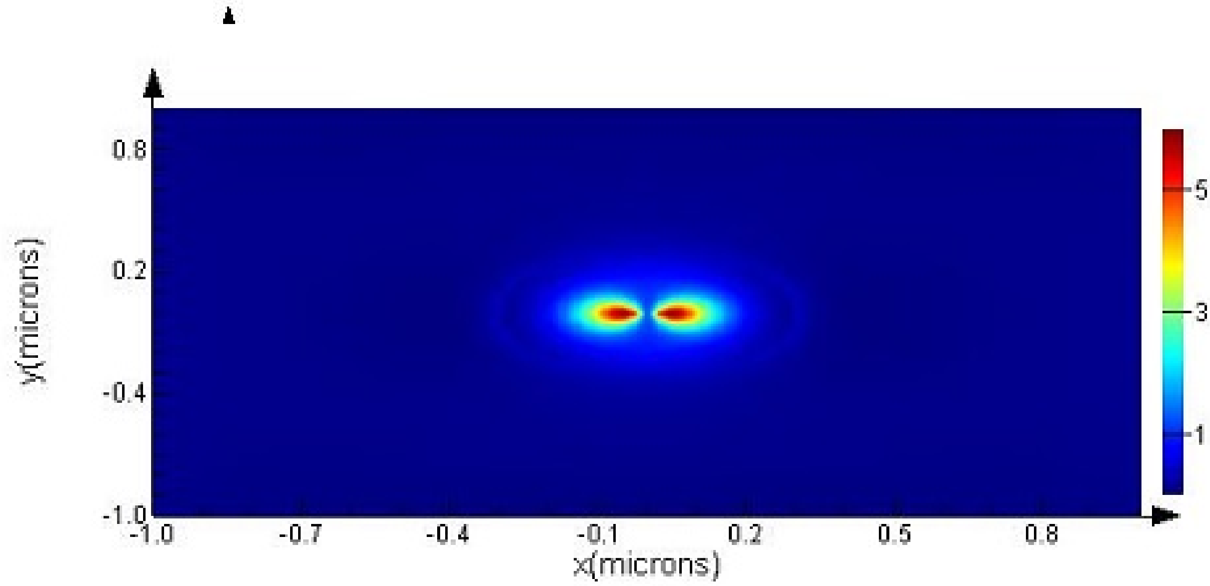

Figure 3. Electrical field located in the middle of silicon cylinder

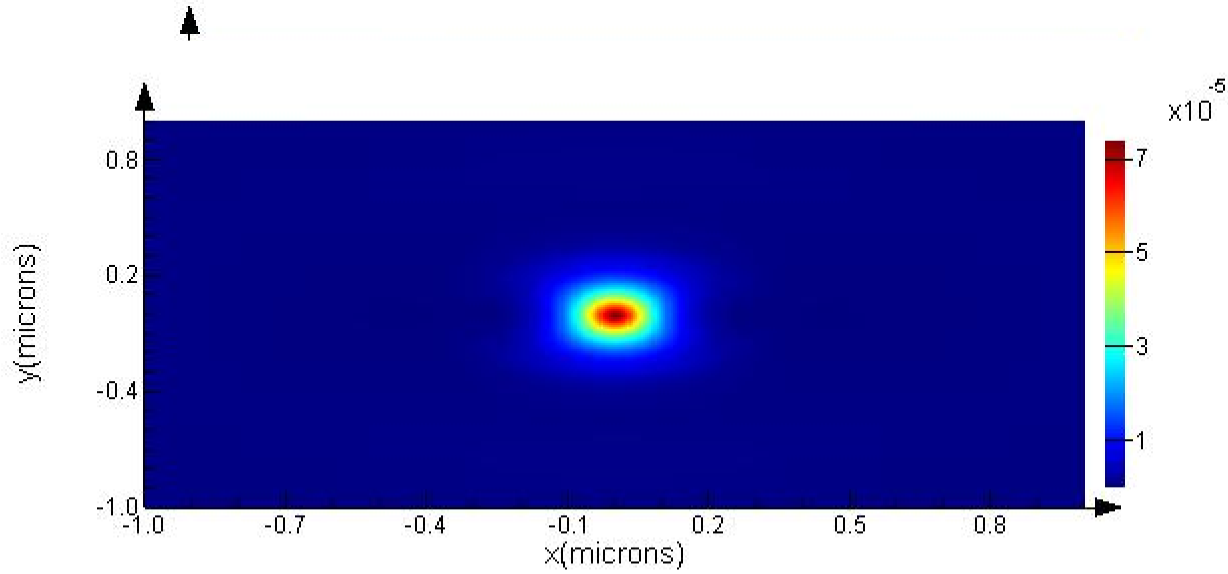

Figure 4. Magnetic field located in the middle of silicon cylinder

2. Conclusion

A silicon photonic integrated nano cavity is designed and theoretically simulated in this work. The 3D FDTD simulation results demonstrate that the nano cavity concentrates and improves the incident optical filed in the interface between the nano cylinder and silicon interface as well in the middle of the nano cylinder.

The photonic silicon technology enables, extends, and increases data transmission. PICs may consume less power and generate less heat than conventional electronic circuits, offering the promise of energy-efficient bandwidth scaling. Silicon Photonic is compatible with CMOS (electronic) fabrication, which allows Silicon Photonic to be manufactured using established foundry infrastructure.

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