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Automatic Voltage Controlled in Two Switch PFC Single Phase Buck Converters

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Abstract — **Conventional single-phase power-factor-correction (PFC) rectifiers with active power decoupling capability typically require more than three active switches in their circuits. By exploring the concept of power-buffer cell, a new single-stage PFC rectifier with two active switches, one inductor and one small power-buffering capacitor is reported in this paper. The proposed converter can achieve high-power factor, wide output voltage range, and power decoupling function without using electrolytic capacitor. Additionally, an automatic power decoupling control scheme that is simple and easy to implement is proposed in this paper. The operating principle, control method, and design considerations of the proposed rectifier are also provided. A 1000-W prototype with ac input voltage of 220 rms and a regulated dc output voltage ranging from 30 to 150 V has been successfully designed and simulated. The simulation results show that with only a 100 µF power-buffering film capacitor, the proposed converter can achieve an input power factor of over 0.99, peak efficiency of 95%, and output voltage ripple of less than 5%, and THD 2% at 1000-W output power.**

Keywords- Automatic power decoupling, capacitance reduction, PFC rectifier, wide output voltage range

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1. INTRODUCTION

Single phase power-factor-correction (PFC) rectifiers have been a preferred solution for a broad range of applications such as power supplies/chargers and lighting because of their circuit simplicity and low system cost. In offline ac to dc power conversion, ripple power of double-line frequency is injected from the ac source into the dc output [1]–[4]. Traditionally, large electrolytic capacitors (E-caps) or large inductors are used at the dc output terminal for buffering the ripple power [4]–[6]. However, an E-cap can take up a significant amount of the system volume (e.g., up to 80% in [7]) and can severely limit system's reliability [8]. Incorporation of active power decoupling control along with a slight modification of the rectifier has been found to be an effective approach that can significantly reduce the capacitance requirement necessary for power buffering [1], [7], [9]–[12]. With these solutions, ripple power can be diverted from the dc output into an external capacitor via an additional power decoupling circuit. Energy (E) stored in a capacitor (C) is $E = 0.5\ CV^2$. By allowing a large voltage (V) across the capacitor, only a small capacitor is required for storing a significant amount of ripple power [1]. Therefore, nonelectrolytic capacitors (non-E-caps) with long lifetime (e.g., film capacitors, ceramic capacitors) can be used with the rectifier circuit in lieu of the E-caps.

The use of active power decoupling in rectifiers seems to work against the principle of system volume reduction. To simplify the circuit structure, several attempts based on circuit integration have been made (e.g.,

component sharing between a PFC rectifier and a power-decoupling circuit [10], [13]). Yet, a minimum of three active switches and two inductors are still needed with such solutions [10]. Some new advancement has been reported in [21], which describes a new two-switch rectifier with active power decoupling capability. The rectifier is compact, reliable, and cost effective. The basic idea of this work is to introduce a type of series power buffer cell into the conventional buck PFC rectifier topology such that two extra operating states are created, i.e., a power charging state and a power discharging state [22], [23]. Power decoupling can therefore be easily achieved via controlling the duration of the two states. One major limitation of this rectifier, however, is that its output voltage range is limited to only half of the peak input voltage. Furthermore, the complementary control scheme used in this rectifier is based on an indirect form of open-loop control involving a complicated power-decoupling loop. In its control, the input ac current and output voltage are not directly regulated (they are not control variables). Instead, only the voltage of the power-buffering capacitor is directly controlled. The duty cycle commands are derived based on complicated open loop calculations using measurements of the power-buffering capacitor voltage, the inductor current, the input voltage and the referenced (desired) output voltage information. Even with such complexity, however, the control is unable to provide accurate regulation of the output voltage and the instantaneous power stored by the power-buffering capacitors.

In this paper, the concept of series power buffer cell is further explored. By rotating the basic circuit cell in [21], a new type of two-switch buck PFC rectifier is derived. This rectifier can achieve good PFC, output voltage regulation, and power decoupling capabilities, all in a single stage. As compared to previous work presented in [21], the proposed rectifier has a new feature of having a wide output voltage range. Furthermore, a novel closed-loop control scheme that can directly regulate the input current and output voltage is proposed. It should be emphasized that, different from all existing control schemes employed in a rectifier with an active power decoupling function, the proposed control scheme achieves automatic power decoupling without a power decoupling loop. This enables a low cost controller to be used in the design. The feasibility of the newly modified two switch rectifier together with the automatic decoupling control is verified through both simulation on a 1kW prototype using a 100 μF long-lifetime non-E capacitor.

*2. **OPERATING PRINCIPLES***

The conventional converter has a low-cost structure because this converter requires only one switching device and five diodes. However, the buck PFC converter fails to provide a sinusoidal waveform for the input current at the zero crossings of the input voltage, i.e., during the period when the input voltage is lower than the output voltage, the total harmonic distortion (THD) of the input current and the output voltage ripple become higher because of the discontinuous current of the smoothing inductor. Therefore, a large smoothing inductor is required in order to obtain a low-THD input current and a low-ripple output dc voltage.

Fig. 1 shows the circuit configuration of the proposed converter. The buffer circuit consists of two switching devices (Swa and Swb), a diode, and a small capacitor. The power pulsation generated with twice the power supply frequency is absorbed by the active buffer capacitor Cdc. If film capacitors or laminated ceramic capacitors can be used, the converter lifetime can be increased, because the lifetimes of these capacitors are longer than that of the electrolytic capacitor. The passive components of the converter without Cdc are only required at the input and output filters in order to eliminate the switching frequency. In this paper, a high-speed switching device MOSFET is selected in order to reduce the filter size.

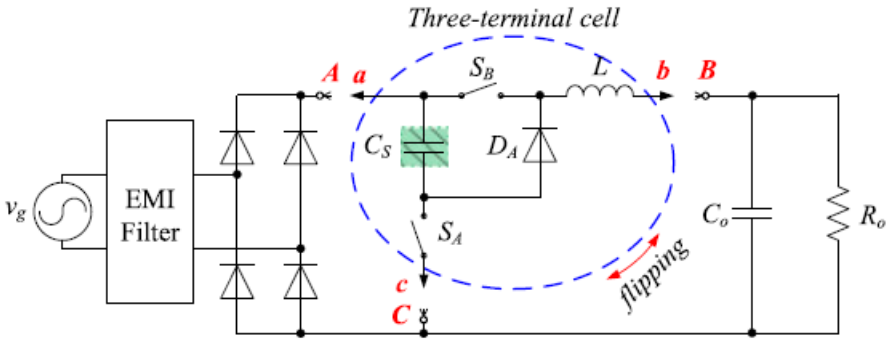

Figure 1. Circuit configuration of the proposed converter.

Table. 1 illustrates the switching pattern of the proposed circuit. The current path does not occur from the rectifier to the active buffer capacitor through the switch Swa because the active buffer capacitor voltage must be higher than the input voltage. Therefore, assuming that the output inductor current is maintained to be constant, the current paths of the proposed converter have four modes based on the switching pattern. In mode 1, the output power is directly supplied by an input single phase source. The buffer power is controlled by modes 2 and 3. In mode 2, the buffer capacitor is discharged. In contrast, in mode 3, the buffer capacitor is charged. Mode 4 is a pass mode of the output inductor current. Thus, the proposed converter performs the function of a buck chopper (modes 1 and 4) and the buffering function of the power pulsation (modes 2 and 3).[11-14]

Operating State	S_A	S_B	C_S	L
State 1	0	1	Idle	Charge
State 2	1	0	Idle	Discharge
State 3	0	0	Charge	Discharge
State 4	1	1	Discharge	Charge

Table. 1: Switching pattern of each mode

3. *OPERATING STATES*

The converter is controlled by four modes, as shown in Table. 1. By employing two active switches and assuming a continuous-conduction-mode of operation, the rectifier has four operation states. They are depicted in Fig. 2 as State 1–State 4. During State 1, the inductor L is charged by the input voltage |vg | and during State 2, it is discharged to the load (Co and Ro). This process is identical to that of a conventional buck boost converter since the power-buffering capacitor CS is in idle mode. In State 3 and State 4, CS is a part of the power flow path and can operate actively to store and release energy. More specifically, CS is charged by the inductor current in State 3, while CS is discharged to the load in State 4. By controlling the duration of State 3 (capacitor charging state) and State 4 (capacitor discharging state), active power decoupling of the ripple power with CS is viable. Table I summarizes the corresponding charging/discharging states of CS and L with respect to the four switching states.

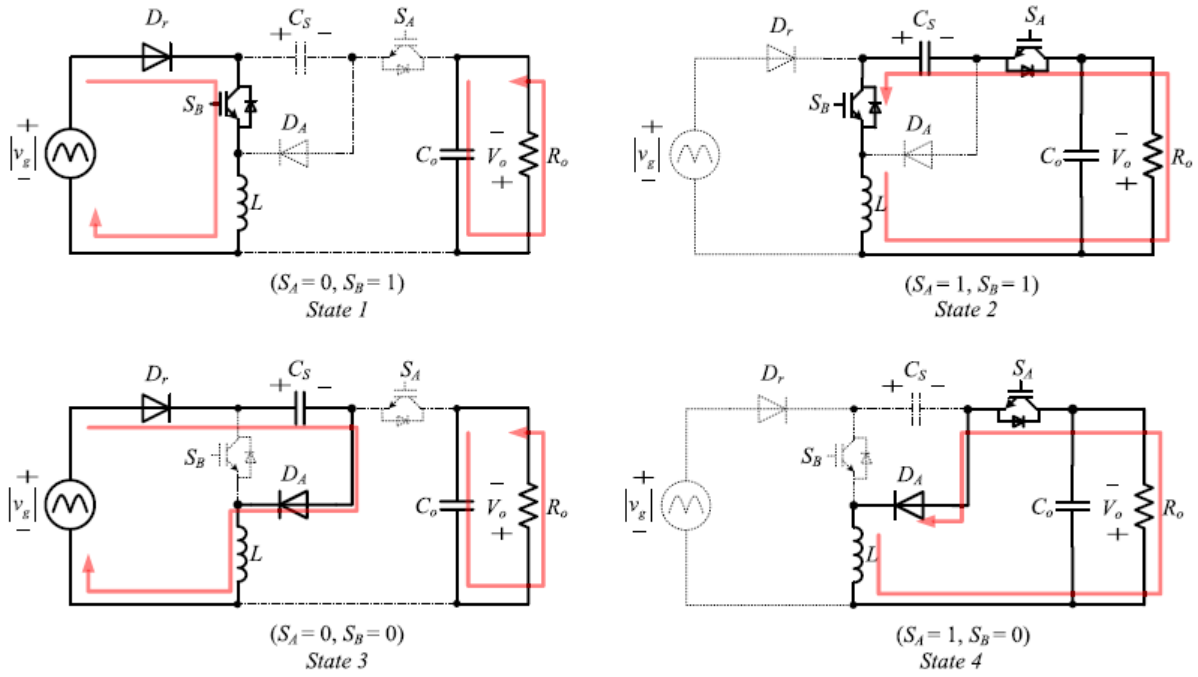

Figure 2. Operating states of the two-switch PFC rectifier in continuous mode of operation.

Assuming that dmode1 through dmode4 are the duty ratios of the respective modes. In order to obtain a sinusoidal input current and dc load current, the duty ratios are constrained as follows:

$$d_{mode1} + d_{mode2} + d_{mode3} + d_{mode4} = 1 \quad (1)$$

$$d_{mode1} + d_{mode3} = \frac{I_{INP}}{i_l} |\sin(\omega t)| \quad (2)$$

$$d_{mode2} - d_{mode3} = d_{tempo} = \frac{v_{out}^*}{v_c} \cos(2\omega t) \quad (3)$$

d_{tempo} has two degrees of freedom, which are decided as follows from the viewpoint of the minimum i_C. When the capacitor current i_C is positive, i.e., when d_{tempo} is positive, mode 2 is selected in order to discharge the capacitor. In contrast, when the capacitor current i_C is negative, i.e., when d_{tempo} is negative, mode 3 is selected. Note that V_{OUT} is usually used as a command to control the converter. Thus, V_{OUT} is replaced by the voltage command V^*_{OUT}. Finally, these duty ratios are given by (1), (2), and (3) in terms of V_{INp}, ω, v_C, and V^*_{OUT}.

4. *PROPOSED CONTROL METHOD*

In this section, we discuss our proposed method to modify duties control as follows:

$$d_{tempo} = \frac{v_{out}^{*}}{v_c}\cos(2\omega t) \qquad (4)$$

Practically speaking, the capacitor voltage does not match the theoretical value due to the voltage error resulting from the ON-state drop of the power device. Thus, the capacitor voltage can be controlled by the PI regulator to the theoretical value[11] but in our proposed method we prefer establish modified d_{tempo} for controlling v_c. Therefore, the theoretical value of the capacitor voltage can be obtained as follows:

$$v_c^{*} = \sqrt{V_{Cmin}^{\ 2} - \frac{P_{out}}{\omega C_{dc}}(\sin(2\omega t) - 1)} \qquad (5)$$

By assuming $\Delta v_c = v_c^{*} - v_c$, we obtain Δd_{tempo} and then modified $d_{tempo}^{\ *}$:

$$\Delta d_{tempo} = \frac{v_{out}^{*}}{\sqrt{V_{Cmin}^{\ 2} - \frac{P_{out}}{\omega C_{dc}}(\sin(2\omega t) - 1)}}\cos(2\omega t) - \frac{v_{out}^{*}}{v_c}\cos(2\omega t) = \frac{\Delta v}{\sqrt{V_{Cmin}^{\ 2} - \frac{P_{out}}{\omega C_{dc}}(\sin(2\omega t) - 1)}}\, d_{tempo} \qquad (6)$$

$$d_{tempo}^{\ *} = d_{tempo} + \Delta d_{tempo} = \left(1 + \frac{\Delta v}{\sqrt{V_{Cmin}^{\ 2} - \frac{P_{out}}{\omega C_{dc}}(\sin(2\omega t) - 1)}}\right) d_{tempo} \qquad (7)$$

Fig. 3 shows a control block diagram of the proposed circuit. Based on (1), (2) and (3), the duty ratio commands are calculated using the detected single-phase voltage v_{in}, the capacitor voltage v_c, the output inductor current i_l, the command of the output voltage V^{*}_{OUT}, the minimum voltage of the active buffer capacitor V^{*}_{Cmin}, and the capacitance of the active buffer capacitor C_{dc}. The gate pulses are given as shown in Table 1. Note that the capacitor voltage is controlled by Δd_{tempo} as a key note for this proposed method based on (4) , (5) , (6) , (7).

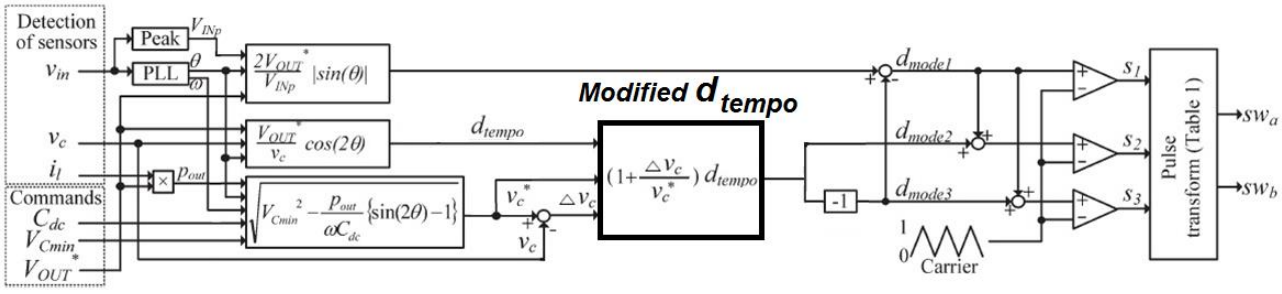

Figure 3. Control block diagram of the proposed method

5 *SIMULATION RESULTS*

In order to demonstrate the validity of the proposed method, a 1kw class prototype circuit has been simulated as Fig. 4 with input RMS voltage 220 V , 50 Hz. Fig. 5 and Fig. 6 shows the operation input and output waveforms of the proposed converter. Based on the results, sinusoidal waveforms without distortion are obtained at the input current. In addition, as shown in Fig. 5 dc waveforms of the output voltage with 5% ripple were obtained. The simulation results reveal that the input current THD is 2% and the input P.F. is over 99%. In addition, a maximum efficiency of over 95% is obtained for a 1kW prototype converter.

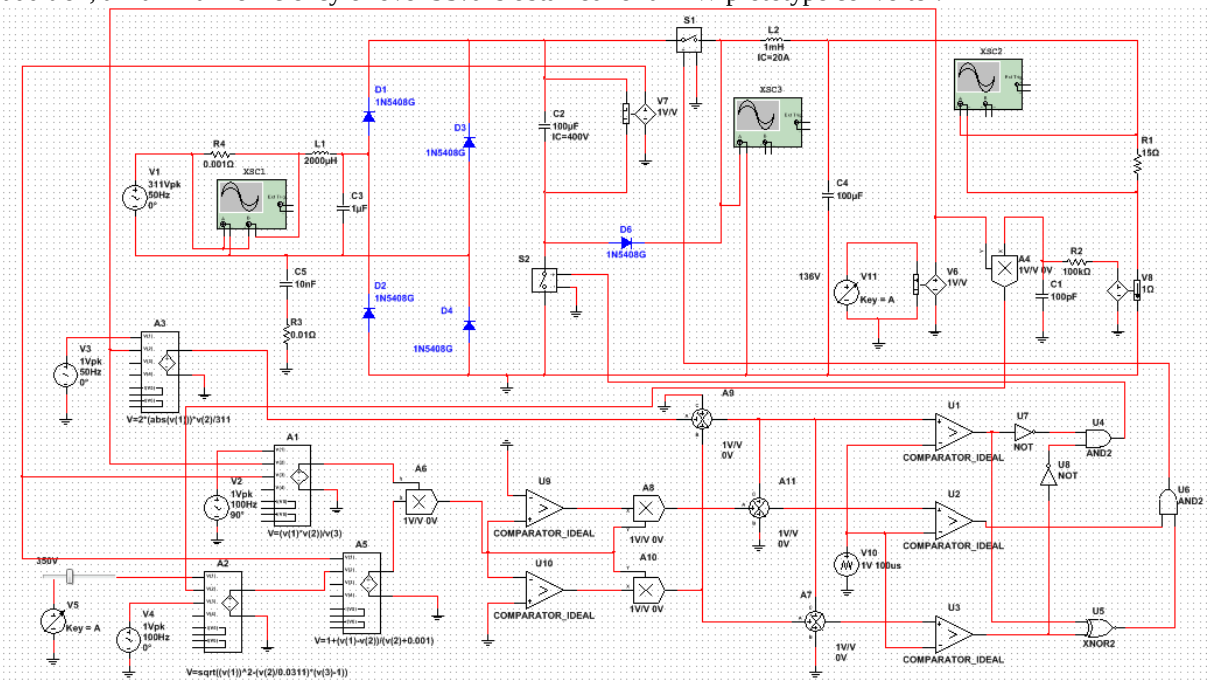

Figure 4. Simulated proposed converter (Vo = 120 V , Po = 1 Kw)

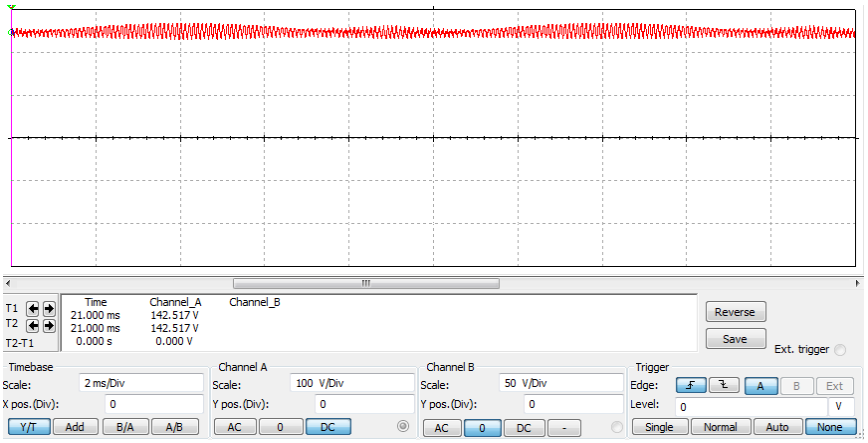

Figure 5. Output Voltage Waveform, Ripple is lower than 5%

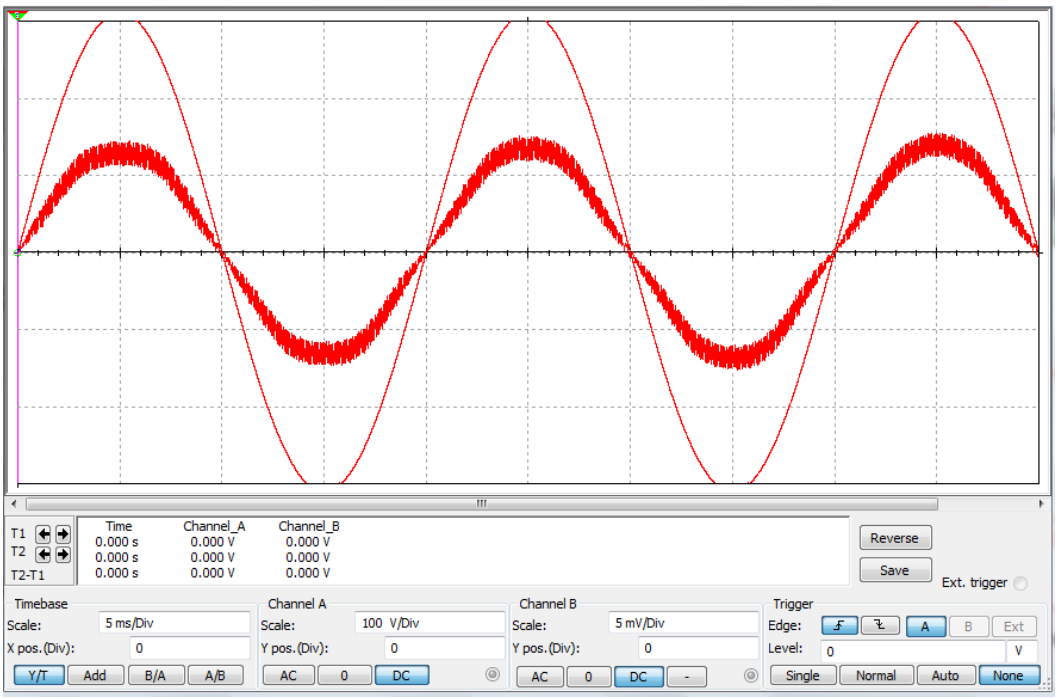

Figure 6. Input Voltage and Current Waveform with THD 2%

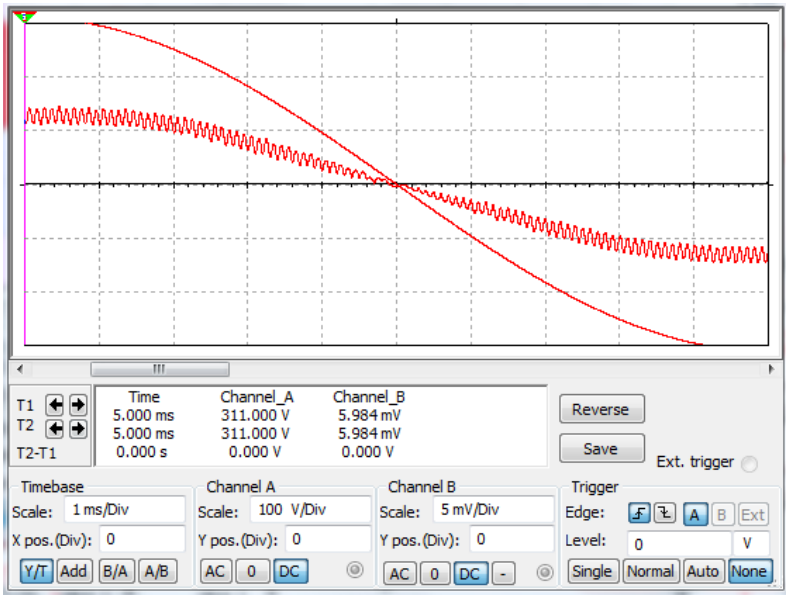

Figure 7. Enlarged Waveform of Figure 6.

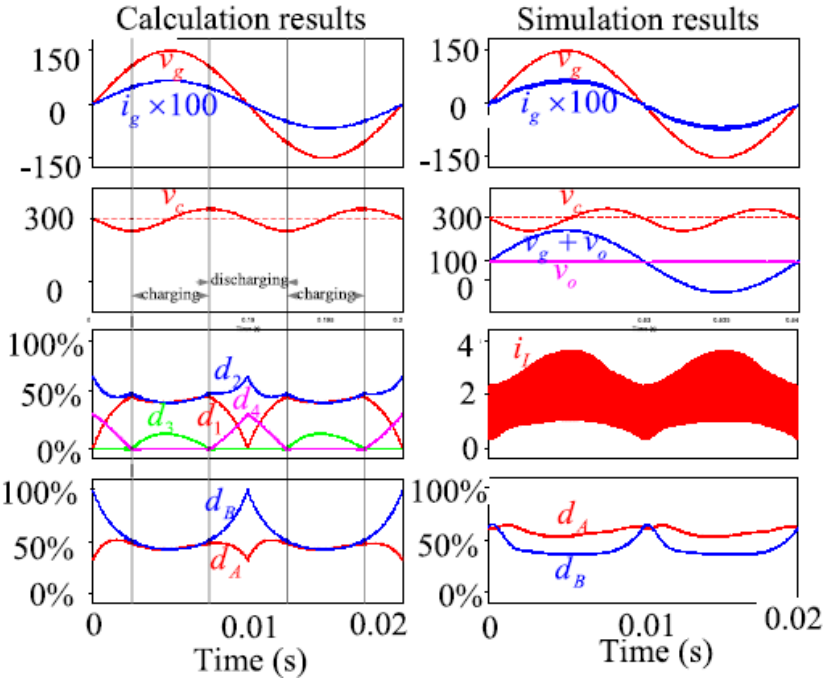

Figure 8. Calculated and (b) simulated waveforms of duty ratios $d_1 - d_4$ and duty cycles d_A and d_B versus the waveforms of ac input voltage v_g, ac input current i_g, and power-buffering capacitor voltage v_c ($d_A=d_2+d_4$, $d_B=d_1+d_4$)

6. *CONCLUSION*

In this paper, a new control method for a two switch PFC rectifier based on the concept of series power buffer cell and the conventional buck converter topology is reported. The rectifier, which comprises only two active switches, one inductor and one small power buffering capacitor, can achieve a high power factor and good voltage regulation over a wide range of output power. In addition, an automatic power decoupling control scheme that is simple to implement and easy to design is proposed for this rectifier. The resulting rectifier is hence simple, cost effective, and reliable. Simulation results show that a peak efficiency of 95% is achievable, with a power factor of higher than 0.99 and a THD of less than 2%. Also, a mere of 5% voltage ripple has been achieved in a 1kW prototype with a 100 μF non-E-cap. We have herein proposed a control method for a single-phase ac–dc converter with a simplified control method in active buffer, which is used to decouple the power pulsation between the input and output sides. The proposed method can achieve low THD at the input current and can also control the low output dc voltage ripple, while our proposed control method has fewer complexity rather than others revealed in references.

References

[1] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4690–4698, Nov. 2012.
[2] T. Shimizu, T. Fujita, G. Kimura, and J. Hirose, "A unity power factor PWM rectifier with DC ripple compensation," IEEE Trans. Ind. Electron., vol. 44, no. 4, pp. 447–455, Aug. 1997.
[3] S. Li, S.-C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. Hui, and C. Tse, "A survey, classification and critical review of light-emitting diode drivers," IEEE Trans. Power Electron., vol. 31, no. 2, pp. 1503–1516, Feb. 2015.
[4] S. Y. Hui, S. N. Li, X. H. Tao,W. Chen, andW.M. Ng, "A novel passive offline LED driver with long lifetime," IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2665–2672, Oct. 2010.
[5] W. Chen, S. N. Li, and S. Y. R. Hui, "A comparative study on the circuit topologies for offline passive light-emitting diode (LED) drivers with long lifetime&high efficiency," in Proc. 2010 IEEE Energy Convers. Congress Expo., 2010, pp. 724–730.
[6] C. K. Lee, S. Li, and S. Y. R. Hui, "A design methodology for smart LED lighting systems powered by weakly regulated renewable power grids," IEEE Trans. Smart Grid, vol. 2, no. 3, pp. 548–554, Sep. 2011.
[7] R. Wang et al., "A high power density single-phase PWM rectifier with active ripple energy storage," IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1430–1443, May 2011.
[8] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications in power electronic converters—An overview," IEEE Trans. Ind. Appl., vol. 50, no. 5, pp. 3569–3578, Sep. 2014.
[9] H. Wang, H. S.-H. Chung, and L. Wenchao, "Use of a series voltage compensator for reduction of the DC-link capacitance in a capacitor supported System," IEEE Trans. Power Electron., vol. 29, no. 3, pp. 1163–1175, Mar. 2014.
[10] S. Wang, X. Ruan, K. Yao, S.-C. Tan, Y. Yang, and Z. Ye, "A flicker free electrolytic capacitor-less AC–DC LED driver," IEEE Trans. Power Electron., vol. 27, no. 11, pp. 4540–4548, Nov. 2012.
[11] Y. Ohnuma and J.-I. Itoh, "A novel single-phase buck PFC AC–DC converter with power decoupling capability using an active buffer," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1905–1914, May 2014.
[12] M. Chen, K. K. Afridi, and D. J. Perreault, "Stacked switched capacitor energy buffer architecture," IEEE Trans. Power Electron., vol. 28, no. 11, pp. 5183–5195, Nov. 2013.
[13] T. Shimizu, Y. Jin, and G. Kimura, "DC ripple current reduction on a single-phase PWM voltage-source rectifier," IEEE Trans. Ind. Appl.,vol. 36, no. 5, pp. 1419–1429, Sep./Oct. 2000.
[14] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," IEEE Trans. Power Electron., vol. 28, no. 3, pp. 1308–1319, Mar. 2013.
[15] M. Su, P. Pan, X. Long, Y. Sun, and J. Yang, "An active power-decoupling method for single-phase AC–DC converters," IEEE Trans. Ind. Informatics, vol. 10, no. 1, pp. 461–468, Feb. 2014.
[16] W. Cai, L. Jiang, B. Liu, S. Duan, and C. Zou, "A power decoupling method based on four-switch three-port DC/DC/AC converter in DC microgrid," IEEE Trans. Ind. Appl., vol. 51, no. 1, pp. 336–343, Jan. 2015.
[17] S. Li, G.-R. Zhu, S.-C. Tan, and S. Y. R. Hui, "Direct AC/DC rectifier with mitigated low-frequency ripple through inductor-current waveform control," IEEE Trans. Power Electron., vol. 30, no. 8, pp. 4336–4348, Aug. 2015.
[18] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," IEEE Trans. Power Electron., vol. 30, no. 6, pp. 2905–2910, Jun. 2015.
[19] S. Li, W. Qi, S.-C. Tan, and S. Y. R. Hui, "Integration of an Active Filter and a Single-Phase AC/DC converter with reduced capacitance requirement and component count," IEEE Trans. Power Electron., vol. 31, no. 6, pp. 4121–4137, Jun. 2016.
[20] W. Qi, H. Wang, X. Tan, G. Wang, and K. D. T. Ngo, "A novel active power decoupling single-phase PWM rectifier topology," in Proc. IEEE Appl. Power Electron. Conf. Expo., 2014, pp. 89–95.
[21] S. Li, W. Qi, S.-C. Tan, and S. Y. Hui, ''Enhanced Automatic-Power Decoupling control method for single-phase AC-to-DC converters,'' IEEE Trans. Power Electron., vol. 33, no. 2, pp. 1816–1828, Feb. 2018.
[22] S. Li, W. Qi, J. Wu, S.-C. Tan, and S.-Y. Hui, ''Minimum active switch requirements for single-phase PFC rectifiers without electrolytic capacitors,'' IEEE Trans. Power Electron., vol. 34, no. 6, pp. 5524–5536, Jun. 2019.
[23] Y. Zheng, K.M. Smedley, Analysis and design of a single switch high step-up coupled-inductor boost converter, IEEE Trans. Power Electron. 35 (1) (2020) 535–545.