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Comparison Of the T-Type Converter and the Conventional 2LVSI for the 60^{kW} Traction Application

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Abstract
The demand for lightweight converters with high control performance and low acoustic noise, increased the switching frequencies of two-level low-voltage 3-phase converters over the last few years. For high switching frequencies, converter efficiency suffers and can be kept high only by employing cost-intensive switch technology such as SiC diodes or CoolMOS switches; therefore, conventional IGBT technology still prevails. In this paper, the alternative of using three-level T-type inverter for low-voltage applications is addressed, and the performance and competitiveness of the T-type inverter, in contrast with conventional two-level voltage source inverters in the same switching frequency, are analyzed in detail. The proposed systems are implemented to connect to a Permanent Magnet Synchronous Motor (PMSM), and Space Vector Modulation (SVM) is applied to the control circuits. The T-type converter basically combines the positive aspects of the two-level converter, such as low conduction losses, small part count, and a simple operation principle, with the advantages of the three-level converter, such as low switching losses and superior output voltage quality. Therefore, it is considered a natural alternative to two-level converters for specific applications.

Keywords: T-type Inverter, Space Vector Modulation (SVM), Permanent Magnet Synchronous Motor (PMSM), Two-Level Voltage Source Inverter (2LVSI)

I. Introduction

Efficient energy conversion in the low-voltage range has gained more and more attention. Applications such as photovoltaic grid inverters, PFC rectifiers, and automotive inverter systems demand outstanding efficiency at low costs. Hence, this paper analyzes the competitiveness of the three-level T-type converter in contrast to conventional two-level converters for low-voltage applications in 10kHz frequency. Compared to the Two-level voltage source inverters (2LVSI), the T-type employs an active bidirectional switch to the dc-link voltage midpoint and gets along with two diodes less per bridge leg. It is an alternative to more complex three-level topologies such as active neutral point clamped converters or split-inductor converters [1,2,3]. The T-type converter basically combines the positive aspects of the two-level converter, such as low conduction losses, small part count, and, therefore, a smaller size to implement, and also a simple operation principle with the advantages of the three-level converter, such as low switching losses and superior output voltage quality. In addition, each bidirectional switch to the DC-link neutral point has to withstand only half of the DC-link voltage making the use of lower-voltage components feasible [4-7].

The paper is organized as follows: section II is devoted to the presentation of a three-phase three-level T-type inverter, and conventional 2LVSI, while section III shows the mathematical model, and section IV explains in detail the principle of the SVM technique. Then, section V shows the simulation and the implementation of the two-level VSI and three-level T-type inverter based on the SVM algorithm respectively, and section VI draws a comparison between 2LVSI and T-type inverters. Finally, the paper ends up with a conclusion in section VII.

II. T-type inverters and conventional 2LVSI

In this paper a three level T-type inverter is selected to compare with traditional two-level voltage source inverters (VSI). The three-level T-type inverter structure is shown in Figure 1. Each leg contains four active switches S1 to S4 with their antiparallel diodes, resembling the shape of the related character “T”.

A positive voltage level +Vdc/2 (P) is performed by turning on the switches S1 and S3, S3 and S4 for the neutral (O) and S2 and S4 for the negative voltage level -Vdc/2 (N) [cf., Table 1].

In the two-level conventional VSI each leg consists of two active switches, and therefore zero voltage state is not formed in this system as shown in Figure 2 [8,9,10].

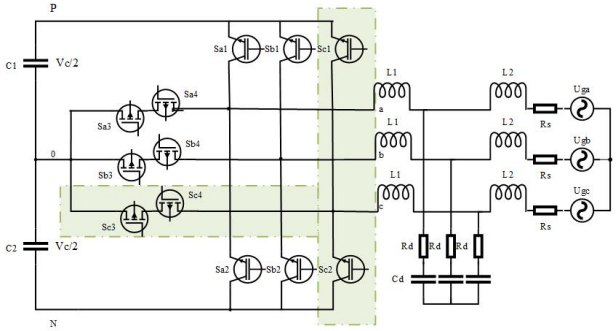

Figure 1 Three-level T-type inverter topology

Table. 1 Switching states for a three-phase three-level T-type inverter

States	Switching states				Terminal Voltage
	Sx1	*Sx2*	*Sx3*	*Sx4*	
P	ON	OFF	ON	OFF	Vdc/2
O	OFF	OFF	ON	ON	0
N	OFF	ON	OFF	ON	-Vdc/2

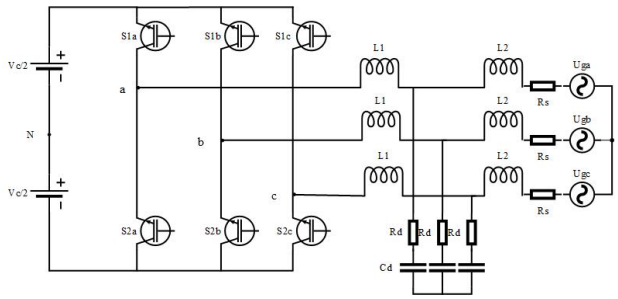

Figure 2 Two-level voltage source inverter (2LVSI)

III. MATHEMATICAL MODEL

The main circuit topology of T-type three-level energy storage inverter is shown in Figure 1 Where, u_{ga} , u_{gb} , u_{gc} are three-phase voltages; U_{dc} is DC voltage; C_1 and C_2 are DC side capacitors (which are not considered in the simplified model), and C_1=C_2=C, U_{dc1}=U_{dc2} ; u_{oa}, u_{ob}, u_{oc} are bridge arm phase voltages; L_1 is output filtering inductor of inverter; C_d is filter capacitor; R_d is damping resistance; L_2 is inductance of load side; R_s is the system resistance; i_{oa}, i_{ob}, i_{oc} are out phase currents of inverter; i_{ga}, i_{gb}, i_{gc} are phase currents while grid-connected operation. The IGBT and anti-parallel diodes of each phase are represented by three-direction switching function S_p, S_o and S_n [11].
Where:

$$\begin{cases} S_{ap} + S_{ao} + S_{an} = 1 \\ S_{bp} + S_{bo} + S_{bn} = 1 \\ S_{cp} + S_{co} + S_{cn} = 1 \end{cases} \tag{1}$$

For brevity, the equations are written only for one phase (the other phases are calculated similarly)
The voltage equation is:

$$L_s\left(\frac{di_{oa}}{dt}\right) = -u_{ga} - R_s i_{oa} + u(S_a, o) + u(o, N) \tag{2}$$

Where, Ls is the reactance of the system, and Ls=L1 + L2. First phase of the three-phase AC output voltages of the inverter is:

$$u(S_a, o) = S_{ap} u_{dc1} - S_{an} u_{dc2} \tag{3}$$

u(o,N) is expressed as follow:

$$u(o, N) = -\left(\frac{u[\![(S]\!]_a, 0) + u(S_b, o) + u(S_c, o)}{3}\right) + \left(\frac{u_{ga} + u_{gb} + u_{gc}}{3}\right) \tag{4}$$

u(S_a,N) is expressed as:

$$u(S_a, N) = \left(S_{ap} - S_p\right) u_{dc1} + (-S_{an} + S_n) u_{dc2} \tag{5}$$

$$u_{ga} + u_{gb} + u_{gc} = 0\,, \begin{Bmatrix} S_{P=} \dfrac{s_{ap} + s_{bp} + s_{cp}}{3} \\ s_n = \dfrac{s_{an} + s_{bn} + s_{cn}}{3} \end{Bmatrix} \tag{6}$$

According to Kirchhoff current law, there are:

$$\begin{pmatrix} L_s\left(\frac{di_{oa}}{dt}\right) \\ L_s\left(\frac{di_{ob}}{dt}\right) \\ L_s\left(\frac{di_{oc}}{dt}\right) \\ C\left(\frac{du_{c1}}{dt}\right) \\ C\left(\frac{du_{c2}}{dt}\right) \end{pmatrix} = \begin{pmatrix} -R_s & 0 & 0 & S_p^* & S_n^* \\ 0 & -R_s & 0 & S_p^* & S_n^* \\ 0 & 0 & -R_s & S_p^* & S_n^* \\ -S_{ap} & -S_{bp} & -S_{cp} & 0 & 0 \\ S_{an} & S_{bn} & S_{cn} & 0 & 0 \end{pmatrix} * \begin{pmatrix} i_{oa} \\ i_{ob} \\ i_{oc} \\ u_{dc1} \\ u_{dc2} \end{pmatrix} + \begin{pmatrix} -\frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 \\ \frac{1}{3} & -\frac{2}{3} & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & -\frac{2}{3} & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{pmatrix} * \begin{pmatrix} u_{ga} \\ u_{gb} \\ u_{gc} \\ i_{dc} \end{pmatrix} \tag{7}$$

Where:

$$S_P^* = \frac{2S_{ap} - S_{bp} - S_{cp}}{3}$$
$$S_n^* = \frac{-2S_{an} + S_{bn} + S_{cn}}{3} \tag{8}$$

IV. SPACE VECTOR MODULATION

Space vector modulation (SVM) is one of the preferred real-time modulation techniques widely used to control voltage source inverters. The three states (P), (O), and (N) in Table. 1 represent the operation of the SVM technique. Considering the operation of three legs, the inverter has 27 possible switching states. There are 24 active and three zero vectors (PPP, OOO, NNN), which lie at the center of the hexagon. The area of the hexagon can be divided into six sectors (A to F), for each has four regions (1 to 4), with 24 regions of operation in total, as illustrated in Figure 3 [12-15].

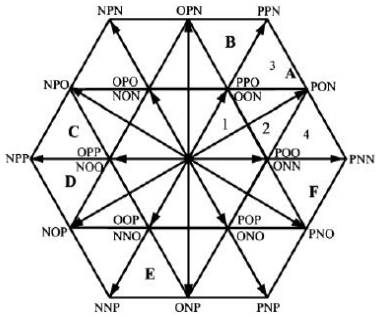

Figure 3 Space vector diagram of the three-level converter [14]

Table. 1 Design Specification

Three-level T-type inverter		Two-level VSI	
Input Voltage (V_{dc})	V_{dc1} =$V_{dc/2}$ =400^{v} V_{dc2} =$V_{dc/2}$ =400^{v}	**Input Voltage (V_{dc})**	800^{v}
P $_{Load}$	60^{kw}	**P $_{Load}$**	60^{kw}
Current (I)	76.89^{A}	**Current (I)**	76.89^{A}
Switching frequency	10^{khz}	**Switching frequency**	10^{khz}
Carrier Frequency	50^{Hz}	**Carrier Frequency**	50^{Hz}
Switch model	Infineon IGBT 600 V, 100 A F3L100R07W2H3 /GaN Systems 650 V E-mode GaN transistor	**Switch model**	Infineon IGBT 1200 V, 150 A F3L150R12W2H 3
load	Dyneo PMSM LSRPM280SD	**load**	Dyneo PMSM LSRPM280SD

V. SIMULATION

For better comparison modeling and simulation have been done using MATLAB/Simulink under the same switching frequency (10^{kHz}) and load (60^{kw}). The Simulink output waveforms equivalent to a three-level T-type inverter and two-level VSI are shown in Figures 4, 5, 6,7. Designed system specification and input date are mentioned in Table 2. The proposed control method is programmed using both MATALB function blocks and logical block diagrams.

Total harmonic distortion (THD) is the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency [16,17]. The measurement of the THD present in the voltage and current signals of the two discussed topologies is shown as follows; Figures 8, 9, 10, 11.

The results of the simulation can be examined in the following areas:

- As it is explicit from Figures 5 and 7, the output phase voltage waveform has improved from the two-level mode in the traditional two-level VSI to the five-level mode in the T-type converter.

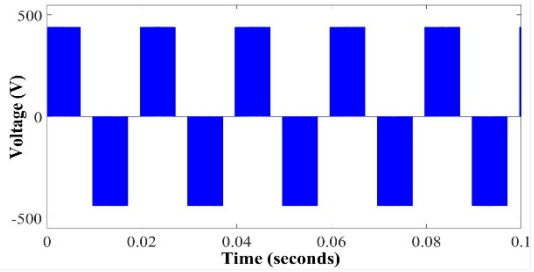

Figure 4 2L-NPC output line to line voltage waveforms

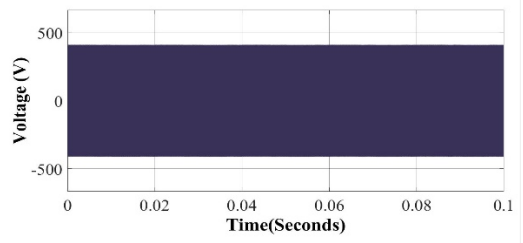

Figure 5 2L-NPC output phase voltage waveforms

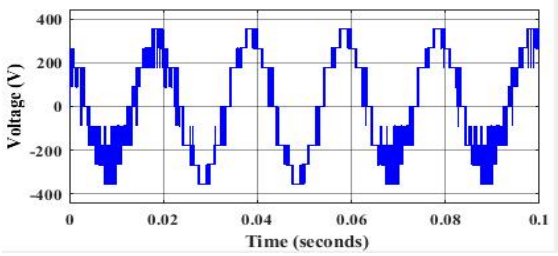

Figure 6 T-type output line to line voltage waveforms

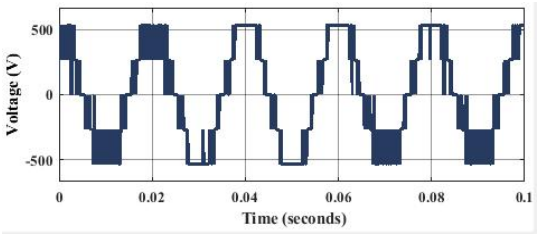

Figure 7 T-type output phase voltage waveforms

- Figures 4 and 6 also show that the output line to line voltage waveform in the traditional two-level converter has improved from three-level to nine-level in T-type.
- The output voltage THD in the T-type converter compared to the traditional VSI model under the same load and switching frequency has improved more than 9 times and has reached 19.33% in the T-type from 180.52% in the traditional 2LVSI. (Figures 8,9)
- In the same way, the THD of the output current in the T-type converter has improved about 2.5 times compared to the traditional VSI model and has reached 17.44% in the T-type from 42.88% in the traditional 2LVSI. (Figures 10,11)

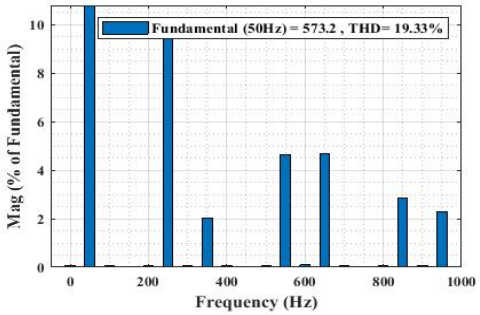

Figure 8 T-type voltage THD

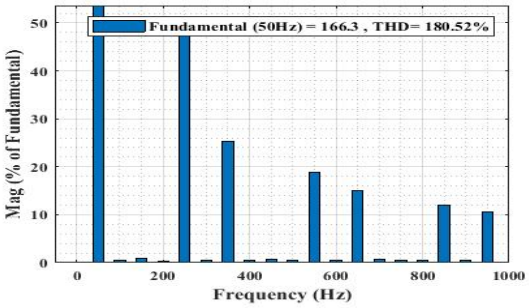

Figure 9 2L-NPC voltage THD

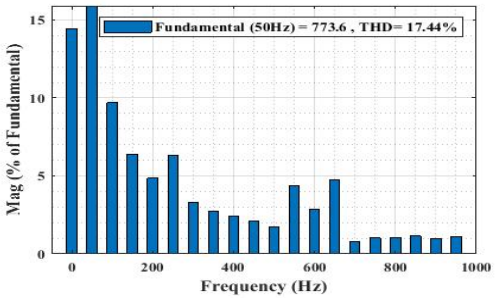

Figure 10 T-type current THD

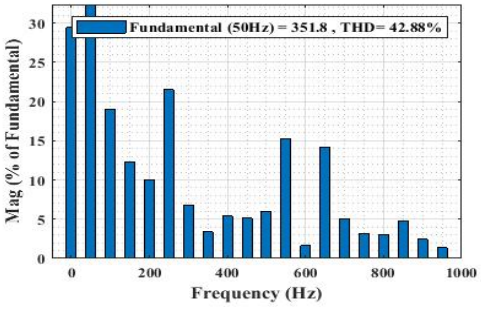

Figure 11 2L-NPC current THD

VI. ANALOGY

The T-type inverter is built with hybrid semiconductor technology. 600^{V} IGBTs/650^{V} GaNs and diodes are combined with 1200^{V} IGBTs and diodes. The current overshoot during the turn-on of T_1 is considerably reduced if the commutating diode is 600^{V} rated compared to the case where the commutating diode is rated for 1200^{V} [cf., Table 3, and Figure 12]. Similarly, the 600^{V} device's turn-off loss energy will be higher [18,19].

Switching losses occur in different semiconductors depending on the switching transition and the direction of the output current. It is essential to analyze the commutation process in detail for every switching transition in order to find what devices obtain turn-on and turn-off losses as well as diode reverse-recovery losses. The implemented space-vector modulation omitted the direct transition from (P) to (N) and vice versa.

Due to the symmetry of the circuit, the turn-on and turn-off energies of both 600^{V} devices are equal under the same conditions (i.e., $E_{T2,on} = E_{T3,on}$, $E_{T2,off} = E_{T3,off}$, $E_{D2,off} = E_{D3,off}$, and $E_{D2,on} = E_{D3,on}$). For the same reason, this also holds for the 1200^{V} devices (i.e., $E_{T1,on} = E_{T4,on}$, $E_{T1,off} = E_{T4,off}$, $E_{D1,off} = E_{D4,off}$, and $E_{D1,on} = E_{D4,on}$) [20,21].

Table 3 summarizes the switching loss energies from the datasheet values. The switching losses will be lower than for the two-level NPC because the commutation voltage is only Vdc/2.

The switching losses increase with higher junction temperature and have been measured at three different temperatures $T_j = \{25^{°C}, 125\ ^{°C}, 150\ ^{°C}\}$.

Also, the conduction losses of each semiconductor device were determined from datasheets. The measured forward characteristics of the 600^{V}, and 1200^{V} IGBT and diode are depicted in Figures 13, and 14 for three different junction temperatures. The typical temperature dependence can be observed. The forward voltage decreases and the differential resistance increases with higher junction temperature.

The semiconductors with higher blocking voltage have higher conduction losses compared to those with lower blocking voltage. The DC link voltage V_{DC} is 800^{V}. It has to be noted that the commutation voltage of the 2LVSI semiconductors is the DC link voltage, whereas of the 3LVSI semiconductors, half the DC link voltage. In order to analyze the losses of each inverter PL_{inv} the following figures (Figures 15, and 16) show the characteristics for different amplitudes of the output currents I, and collector currents I_c [22,23].

Table. 1 Switching loss energy

Component	Switch	Energy	Condition
Infineon IGBT 600 V, 100 A F3L100R07W2H3	$ET_{1,ON}$ $ET_{1,OFF}$	0.469 3.31	V_l=300V I_{out}=100A T_j=125°c
Infineon IGBT 1200 V, 150 A F3L150R12W2H3	$ET_{3,ON}$ $ET_{3,OFF}$	2.1 2.4	V_l=400V I_{out}=75A T_j=125°c

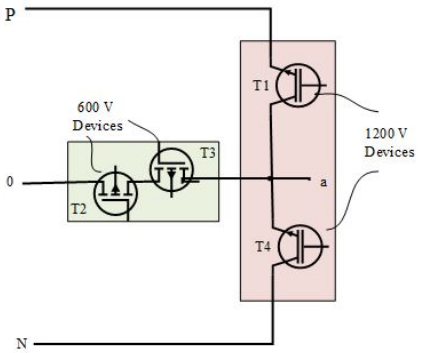

Figure 12 Bidirectional switch to the midpoint can be implemented with two IGBTs or GaN transistors

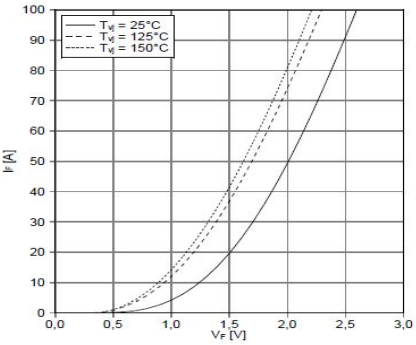

Figure 13 Measured forward voltage drop of the 600^{V} IGBTs for three different junction temperatures [24]

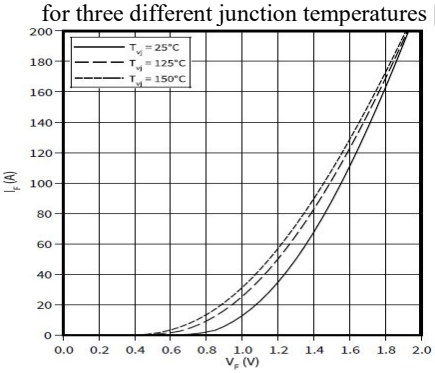

Figure 14 Measured forward voltage drop of the 1200^{V} IGBTs for three different junction temperatures [25]

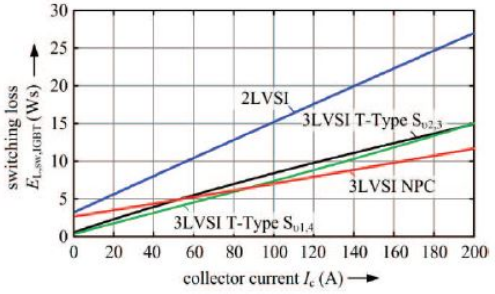

Figure 15 conduction losses [20]

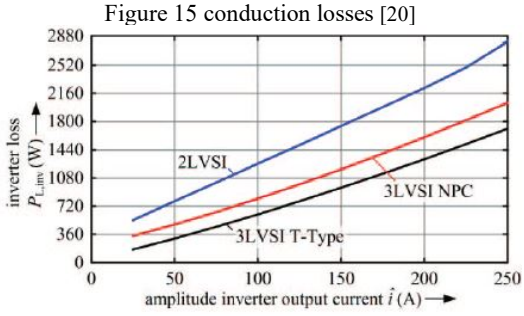

Figure 16 inverter losses [20]

VII. CONCLUSION

A three-phase T-type converter topology is presented and compared with the conventional 2LVSI. The space vector modulation control strategy is applied to both inverters. THD values of the output voltage and current of the systems are measured under the same operating conditions. T-type shows better results in THD analyses than 2LVSI, and successfully improved the voltage THD by about 160% compared to 2LVSI, and also the current THD was improved by 25% compared to THD in 2LVSI. Although the number of active switches in the T-type converter is more than the number of 2LVSI switches, due to the fact that the T-type converter switches are exposed to half of the DC link voltage, it is possible to use lower ranges of components and hence benefit from the lower prices. This compensates the costs in a way, especially for higher power ranges.

To a large extent, the machine losses depend on the inverters´ output current waveforms and their mean current ripple. These influences are described, and the impact of various switching frequencies is depicted. The loss characteristics of two different topologies are examined and presented. In general, the T-Type 3LVSI seems to have a better waveform (in terms of the number of steps and closer to a sinusoidal waveform), more appropriate THD, a lower total loss, and thus higher efficiency.

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