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Comprehensive Investigation on CM Voltage, Bearing Current, and THD in MLI-fed Motor Drives using SPWM

Mohammad Shokrani[1], **Ahmadreza Karami-Shahnani**[2], **Karim Abbaszadeh**[3]

[1] Department of Electrical Engineering, K.N.Toosi University of Technology, Tehran, Iran; Mohammad.Shokrani@email.kntu.ac.ir
[2] Department of Electrical Engineering, K.N.Toosi University of Technology, Tehran, Iran; ar.karami@email.kntu.ac.ir
[3] Department of Electrical Engineering, K.N.Toosi University of Technology, Tehran, Iran; Abbaszadeh@kntu.ac.ir

Abstract
In recent years, multilevel converters have received significant consideration as power-conversion systems for demanding applications requiring high power and power quality. Furthermore, Pulse-width sequences have been recognized as the primary defining factor of common-mode voltage (CMV), which through parasitic capacitances, generate bearing currents and shaft voltages, which are major points of failure for electric drives. This research focuses on carrier-based sinusoidal pulse width modulation strategies for three five-level inverters, including cascade H-bridge (CHB), neutral-point-clamp (NPC), and packed U-cell (PUC). Multilevel inverter-fed motor drive and the equivalent circuit of parasitic capacitances in the inverter-driven motor are modeled and simulated using MATLAB/SIMULINK, and the results are compared and discussed.
Keywords: Bearing current, common-mode voltage (CMV), multi-level inverter (MLI), total harmonic distortion (THD).

Introduction

Multilevel inverters (MLI) have become increasingly popular in a variety of medium- and high-power industrial applications as an effective solution for high voltage/power DC-AC conversion to address the rising demand for more robust power supplies [1]–[4]. Also, due to its capacity to produce voltage and current with lower total harmonic distortion (THD) than traditional two-level inverters, multilevel inverters are becoming more popular in low-voltage applications, too [2]. They are power-conversion systems made up of various power semiconductors and DC voltage sources. When coupled and managed properly, they can produce a multiple-step voltage waveform with variable and controllable frequency, phase, and amplitude [3]. There are a huge number of applications that use MLIs, including variable frequency drives, air conditioning, uninterruptible power supplies, induction heating, high voltage DC power transmission, electric vehicle drives, static var compensators, active filters, flexible AC transmission systems, and DC power source utilization (such as electricity obtained from batteries, solar panels or fuel cells) [4]. Despite efforts to make power converters more effective, the growing usage of these converters in electrical drive systems has renewed worries about one of these systems' primary issues, i.e., the common-mode voltage (CMV) [5].

The CMV results in excessive voltage stress on motor windings, shaft voltage, and subsequently bearing currents, which could lead to premature bearing failure and insulation breakdown. Additionally, the presence of CMV and induced common-mode currents (CMIs) can cause electromagnetic interference (EMI), which can make it difficult for delicate control electronics to function when they are placed close to common-mode (CM) noise channels [2]. The square-wave phase voltages of the pulse-width modulated converter determine the CMV waveform. Due to their low cost and simple implementation, CMV reduction methods based on space vector PWM (SVPWM) or carrier-based PWM (CBPWM) are more applicable when compared to large-size and expensive CMV filters [6], [7]. Theoretically, the SVPWM-based CMV reduction approach can be implemented equivalently by CBPWM by altering the carrier type, injecting zero-sequence voltage (ZSV), or shifting the phase position of PWM pulses. CBPWM is also considerably more straightforward to implement than SVPWM, and a typical strategy to lower CMV is to modify the carrier type [8].

Furthermore, in the context of electrical drives, rolling element bearing failures account for more than 50% of motor failures and are the primary source of downtime [9]. In recent decades, there have been numerous reports of the phenomena of bearing currents when a motor is driven by a Pulse Width Modulation (PWM)Voltage Source Inverter (VSI) which several research have suggested that the common mode (CM) voltage of a PWM inverter is related to the development of bearing currents. In [10]the shaft voltages and bearing currents in rotating machines are reviewed. A bearing current equivalent circuit model has been proposed in [11] for fully understanding the phenomena. Also, the bearing current and shaft voltage mitigation in a five-level Neutral-Point-Clamp (NPC) inverter with three SPWM techniques is analyzed in [12].

Prior research on multilevel inverters was restricted to reducing common mode voltage and bearing current approaches. In this study, a new five-level inverter, Packed-U-Cell (PUC), will be simulated and investigated alongside two conventional multilevel inverters. A thorough investigation has been conducted in order to determine the impact of common mode voltage in multi-level inverters on bearing current, shaft voltages, total harmonic distortion (THD) in line voltages, and electric torque ripple of the induction machine. The performance of the inverters will be analyzed using PD, POD, APOD [13], COPD, COPOD, and COAPOD [14] SPWM techniques, which will be investigated later.

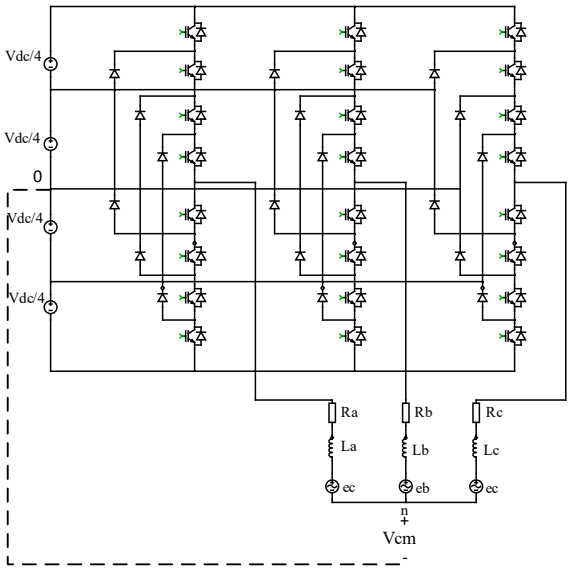


Figure 1. Schematic of five-level NPC induction motor drive

Common Mode Voltage

The phase voltages with respect to the motor's neutral point (assuming a Y connection) in any balanced ac three-phase motor system with purely sinusoidal excitation are made up of only positive sequence components, hence the instantaneous sum of the time-domain phase voltages is zero. Normally, this circumstance applies to motors directly connected to utility mains. The inability to manage the motor speed and torque, which results in less than optimal control and operational efficiency, is the main disadvantage of this scenario. Furthermore, direct-line starting can result in inrush currents more than six times the motor's rated current. Using VSI-based motor drives offer answers to these issues but comes with significant disadvantages due to non-sinusoidal output voltages, and their time-domain phase voltages at any given point during the ac cycle may not sum up to zero [2].

Referring to Figure 1, the inverter three-phase output voltages with respect to the midpoint of the DC bus "0" can be expressed as follows:

$$V_{a0} = V_{an} + V_{n0} \quad (1)$$

$$V_{b0} = V_{bn} + V_{n0} \quad (2)$$

$$V_{c0} = V_{cn} + V_{n0} \quad (3)$$

Combining (1) to (3) and figuring out V_{n0} results in:

$$V_{n0} = \tfrac{1}{3}(V_{a0} + V_{b0} + V_{c0} - (V_{an} + V_{bn} + V_{cn})) \quad (4)$$

If the load is balanced, the line-to-neutral voltages sum up to zero, and CMV can be expressed as:

$$V_{CM} = V_{n0} = \tfrac{1}{3}(V_{a0} + V_{b0} + V_{c0}) \quad (5)$$

Shaft Voltage and Bearing Current

For a long time, shaft-induced voltages that cause

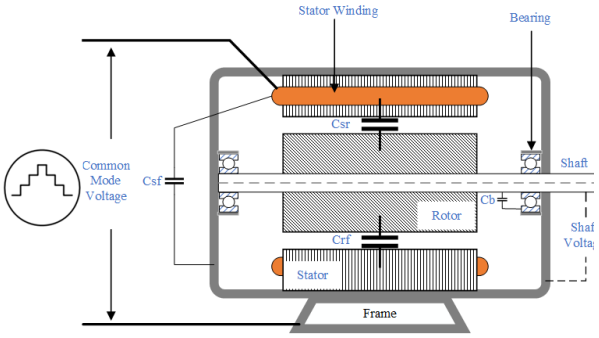


Figure 2. Schematic of parasitic capacitances of an inverter-fed electric motor

bearing currents have been of great concern. Inside the machine, capacitive and inductive coupling produces high-frequency bearing currents. All drive systems have parasitic capacitances and inductances, which are never taken into account while operating with pure sinewaves. It has been discovered that when an inverter is operating, the high-frequency (HF) components of the CM voltage excite the motor's parasitic capacitances and inductances, resulting in what is known as "inverter-induced bearing currents." The numerous parasitic capacitances in an AC motor are depicted in Figure 2 and become important when the motor is powered by a PWM voltage source inverter. The parasitic capacitances depicted in Figure 2 experience pulsed current flow due to the high dv/dt of common mode voltage supplied across the stator and grounded frame of the motor. The variables are dispersed in reality, but for the purposes of analysis, they can be classified into the following four categories [15]:

❖ **Stator winding to rotor capacitance (C_{sr}):** This capacitance is created between the rotor frame and stator winding. Despite having a relatively low value, this capacitance is the main pathway for charging the rotor body, to which the motor shaft is physically attached. Therefore, it is crucial to consider this capacitance's value when determining the shaft voltage's size.

❖ **Rotor to Frame capacitance (C_{rf}):** The charging path from the stator winding to the rotor surface is finished by the rotor-to-frame capacitance. About 10% of CMV appears across this capacitance due to the voltage divider effect. The voltage that developed across C_{rf} is called the "shaft voltage." The capacitance between the rotor and the frame thus determines the shaft voltage.

❖ **Bearing capacitance (C_b):** The shaft speed, lubrication type, ball or roller surface area, temperature of the lubricant, mechanical stress on the shaft, and lubricant temperature all affect how much capacitance is present. This parasitic capacitance is transitory and only appears when the motor rotates. The value of this capacitance is crucial since the bearing's life and bearing current is determined by its properties.

Also, according to the capacitive voltage divider circuit, the shaft voltage can be obtained from the following equation:

$$V_{sh} = \frac{C_{sr}}{C_{sr} + C_{rf} + C_b} V_{CM} \quad (6)$$

Multi-Level Inverters

Due to their numerous advantages, multilevel inverters have emerged as a research hotspot in high-voltage and high-power applications. It is commonly known that one of the main strategies for lowering harmonic content without lowering output power is to create multilevel waveforms.

The two most prevalent multilevel inverters in power electronic medium\high power applications, particularly in industrial adjustable speed drives (ASD), are Neutral-Point-Clamp and Cascade- H-bridge (CHB) converters [3]. Figure 1 shows the schematic of a five-level inverter-fed induction motor drive. Note that, DC-bus voltage unbalancing is one of the significant problems with diode clamped multilevel inverters. because voltage balancing is not an issue with this work, for the DC buses, separate DC sources have been given.

CHBs are multilevel converters created by joining two or more single-phase H-bridge inverters in series. Since each H-bridge or power cell has one redundant switching state, and the series connection naturally introduces more redundancies, CHB provides more redundancies than other well-known inverters like NPC or Flying Capacitor (FC) inverter topologies. These redundancies and the topology's inherent modularity are benefits that make the fault-tolerant operation possible. Another benefit is that since all semiconductors simply need to block V_{dc}, the output voltage and power are effectively increased. The primary disadvantage is that each H-bridge inverter requires a separate DC supply, which is typically provided by a transformer-fed three-phase rectifier. Consequently, a three-phase five-level inverter requires a transformer with six secondary three-phase windings and the associated diode bridges, which increases the converter's size and price[3].

Traditional multilevel architectures like NPC, FC, and CHB have the major drawback of requiring a significant increase in the number of power electronic switches as the number of output voltage levels rises, making the system as a whole complex and expensive. This problem results in decreased reliability, more difficult defect detection, and expensive repair and maintenance. It would be crucial in practice to reduce the number of switches, gate drives, and DC sources employed in the inverter [1]. Recently, a new multilevel inverter topology named Packed U-Cell (PUC) has been introduced with the aim of lowering the number of components in [15]. Each U cell in a PUC inverter consists of two power switches and one capacitor, as shown in Figure 3, providing good power quality with a minimal amount of passive and active parts. It can be categorized as a compromise position between the CHB and FC topologies.

Carrier-based SPWM

Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM), and Selective Harmonic Elimination Pulse Width Modulation (SHEPWM) are the three primary modulation techniques utilized for multilevel inverters [16]. SPWM is simplest of all the above techniques. The fundamental idea behind a multi-carrier SPWM approach is to compare the modulating signal to a multi-carrier waveform of various

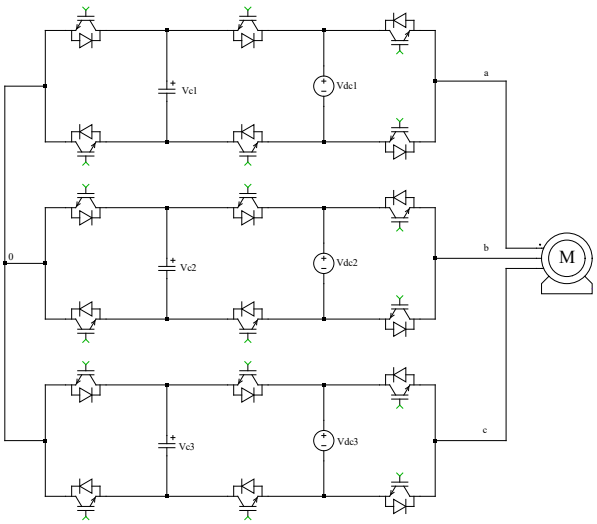


Figure 3. Three-Phase Five Level Packed-U-Cells Converter

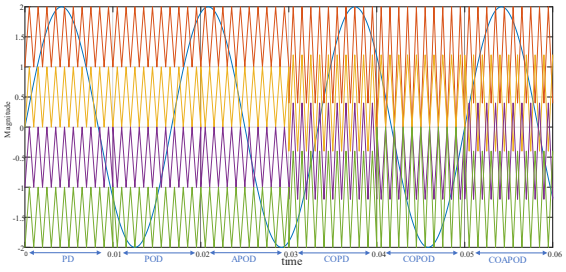


Figure 4. multicarrier non-overlapping and overlapping strategies

levels. The frequency of the carrier signal indicates the switching frequency of an inverter. In a carrier-based SPWM approach for m-level inverters, (m-1) triangular carriers and a single sinusoidal modulating signal are compared. Where m is the inverter's output voltage level [14]. The carrier-based SPWM techniques used in this paper, shown in Figure 4, can be classified into two carrier SPWM strategies: overlapping and non-overlapping strategies. Also, non-overlapping carrier-based SPWM techniques are classified as follows:

❖ **Phase Disposition (PD):** It requires m-1 number of the triangular carrier, which are identical in frequency, amplitude, and phase and are equally displaced with respect to the zero axis.

❖ **Phase Opposition Disposition (POD):** The carrier signals above the sinusoidal reference zero point are 180° out of phase with those below the zero-reference voltage.

❖ **Alternative Phase Opposition Disposition (APOD):** The same-amplitude carrier signals used in the APOD-SPWM approach are 180° out of phase with each other's surrounding carrier signals.

Furthermore, overlapping carrier-based SPWM techniques are classified as follows:

❖ **Carrier Overlapped Phase Disposition (COPD):** In this technique, carriers are overlapped such that the space between each carrier is half the amplitude of the carrier signal.

❖ **Carrier Overlapped Phase Opposition Disposition (COPOD):** In this technique, two groups maintain phase inside the group despite being out of phase with one another.

❖ **Carrier Overlapped Alternative Phase Opposition Disposition (COAPOD):** The amplitude of the carriers

Table 1. Inverters parameters

	CHB	NPC	PUC
No. of switches	6	4	3
No. of Independent dc sources	8	8	6
Dc source voltages (V)	90	90	180
No. of Dc bus capacitances	0	0	3 (6mF)

Table 2. Motor and parasitic capacitances parameters

Motor Parameters		**parasitic capacitances**	
Rated power (HP)	3	**C_{sf} (nF)**	11
Pole pairs	2	**C_{sr} (pF)**	100
Rated Voltage (V)	220	**C_{rf} (nF)**	1.1
Rated Frequency (HZ)	60	**C_b (pF)**	200

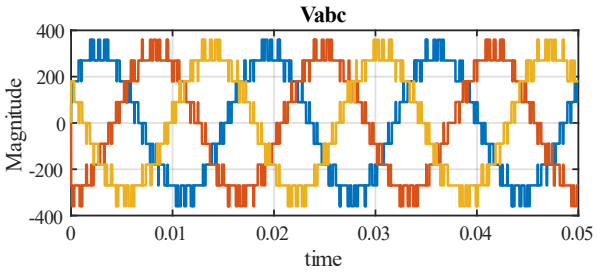
overlaps with nearby carriers that are 180° out of phase with one another.

Results and Discussion

Simulation is carried out using MATLAB/Simulink to examine the performance of each of the inverters under switching using techniques discussed above. The simulated inverters parameters are listed in "Table 1".

Also, the parameters of an induction motor used for motor drive simulation and the values of parasitic capacitances of common-mode equivalent circuit for a PWM inverter-fed motor which are valid for a wide range of induction motor horsepower ratings with typical ball bearings [11] are shown in "Table 2".

In following figures simulation results of a five level Cascade- H-bridge motor drive inverter will be illustrated the three-phase output voltage of inverter (V_{abc}), total-harmonic-distortion of line voltage (THD), common-mode voltage (V_{cm}), shaft voltage (V_{sh}), three-phase current (I_{abc}), bearing current (I_b) and the electrical torque of machine (T_e) under various multicarrier SPWM methods.



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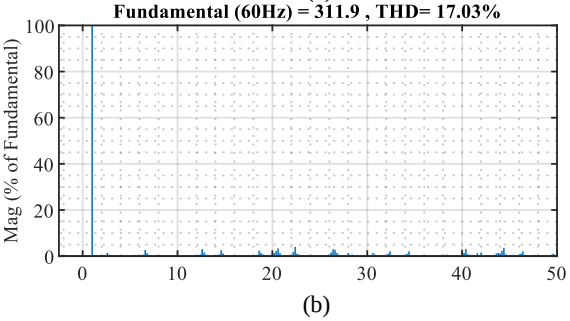

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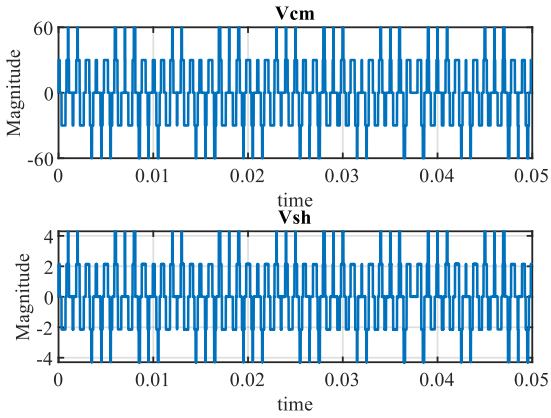

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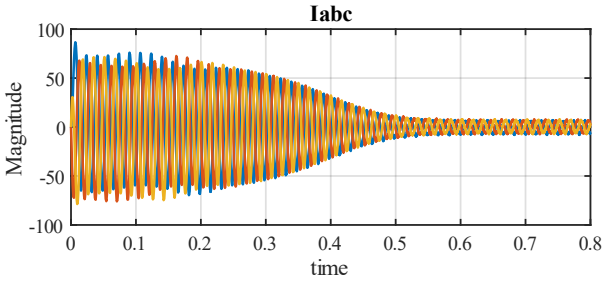

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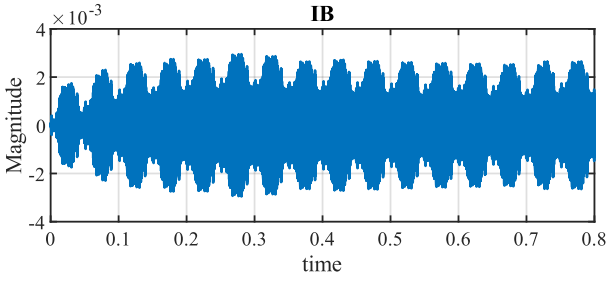

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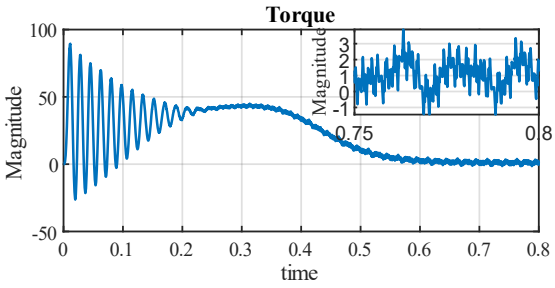
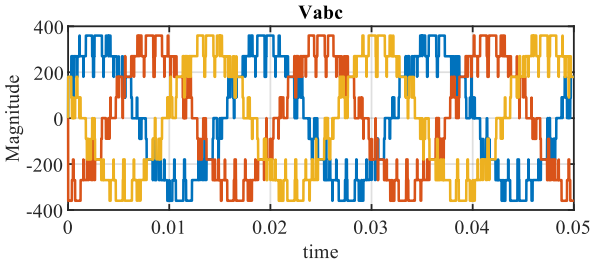


(f)

Figure 3. Simulated time-domain waveforms of CHB motor drive inverter using PD-SPWM. (a) V_{abc}. (b)THD. (c) V_{cm} and V_{sh}. (d) I_{abc}. (e) I_b. (f) T_e

Figure 3 and 4 shows PD-SPWM and COAPOD-SPWM simulation results respectively. Also, "Table 3"



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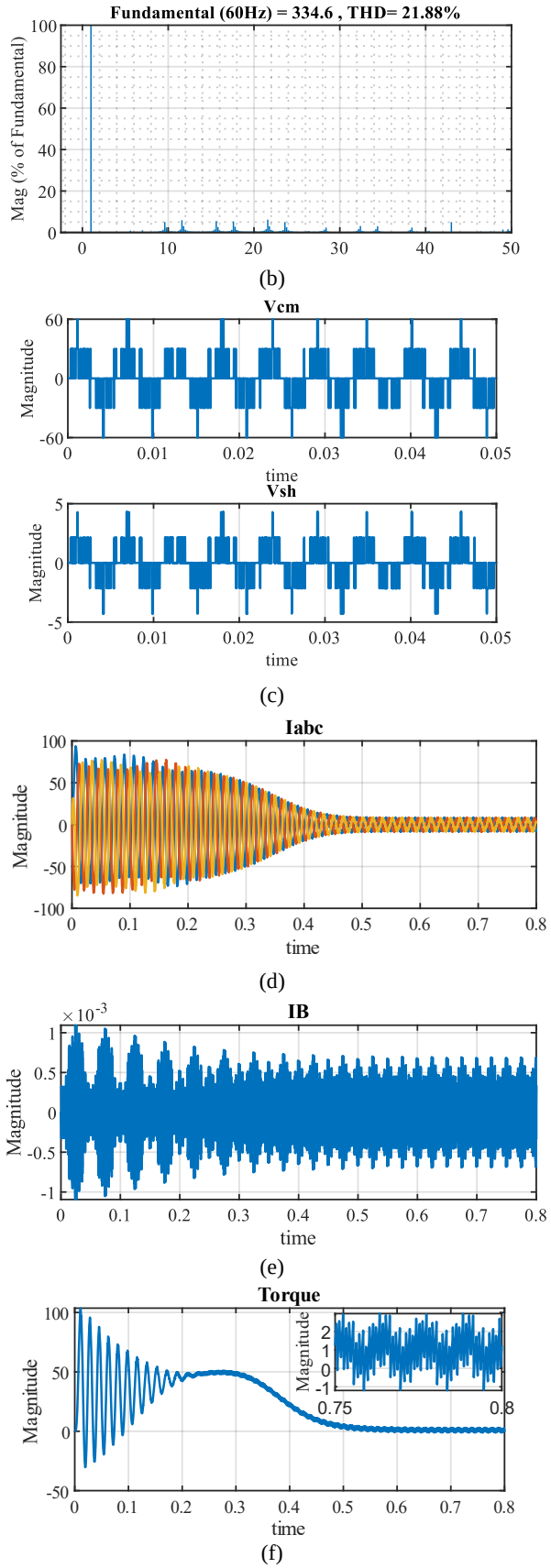

Figure 4. Simulated time-domain waveforms of CHB motor drive inverter using COAPOD-SPWM. (a) V_{abc}. (b)THD. (c) V_{cm} and V_{sh}. (d) I_{abc}. (e) I_b. (f) T_e

summarizes the results obtained by driving the induction motor with three five level inverters using six different modulation techniques mentioned above. By analyzing obtained data, the following can be concluded:

- In all three inverters, the common mode voltage is the lowest after reaching stable conditions with the two methods POD and APOD. Nonetheless, as shown in "Table 3", the peak voltage value of the CMV in the PUC inverter has a higher value before reaching the stable condition, and this is visible in all switching techniques except COPOD and COAPOD. But after the motor reaches a stable condition, the value of the CMV is the same as the previous two inverters, and its lowest value occurs in two POD and APOD methods with the value of Vdc/12. Of course, it should be noted that the obtained data are for *ma*=1, and for *ma*<1, the only POD method remains at Vdc/12 while the peak value of CMV in method APOD increases to the Vdc/6. Figure 5 depicts the CMV peak value of different switching techniques in varus modulation conditions.
- Based on the obtained results, it can be seen that in all cases, THD has an inverse relationship with the common-mode voltage, so that when CMV decreases from Vdc/6 to Vdc/12 in POD and APOD, the value of Line Voltage THD increases up to around 5% and 8% and the current THD increases by about 2% and 6% respectively, which effect of this increment can be seen in the torque ripple. Furthermore, the percentage of THD in PD and COPOD methods has its lowest and highest value, respectively.
- Also, according to the data, it can be seen that torque ripple is not directly related to current THD, and for COAPOD method, which has a higher current THD than PD method, the value of torque ripple is the lowest value among whole methods, thus for applications that less torque ripple is required, the COAPOD method gives better results. It should be mentioned that, although the PD method obtains a lower common-mode voltage, it produces a larger torque ripple than other methods.
- The bearing current has its highest value in COPD method and has the lowest value in COAPOD method. The remarkable thing is that in the PUC inverter, the bearing current has a noticeable drop and its value has decreased significantly. Therefore, the PUC inverter can be a suitable option to reduce the bearing current in electric motor drives.
- Also, the RMS of the output voltage has its highest value in the COPOD method, which can be considered for applications that require a higher voltage RMS.

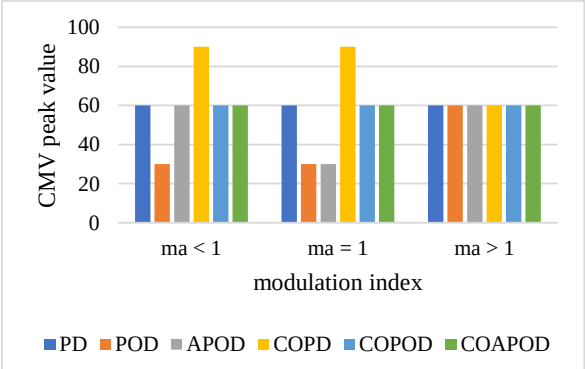

Figure 5. CMV peak value with different modulation index

Table 3. Motor drive simulation results

	CHB						NPC						PUC					
	PD	POD	A POD	CO PD	CO POD	COA POD	PD	POD	A POD	CO PD	CO POD	COA POD	PD	POD	A POD	CO PD	CO POD	COA POD
CMV Peak (V)	60	30	30	90	60	60	60	30	30	90	60	60	69	42	38.8	93.8	60	60
Shaft Voltage Peak (V)	4.3	2.16	2.15	6.5	4.3	4.19	4.3	2.19	2.19	6.17	4.33	4.32	4.9	3.1	2.16	6.7	4.33	4.32
Bearing Current Peak (mA)	2.9	2.16	1.11	16	2.25	1.09	2.9	1.91	1.11	16	2.16	1.12	0.8	0.77	0.61	3	1	0.49
Line Voltage THD (%)	17	21.5	25.2	20	25.3	21.9	17	21.5	25.3	20.18	25.3	23.8	17	21.2	25	21.1	25.2	21.6
Phase Current THD (%)	12	13.9	17.7	12	16.2	14.4	12	13.8	17.7	12.2	16.2	23.4	12	13.6	17.5	17.6	16.2	14.3
Torque Ripple	5.3	7.22	4.56	6.2	6.62	4.19	5.4	7.17	4.57	6.17	6.44	11.4	4.3	7.99	4.77	9.97	6.49	4.07
Line Voltage RMS (V)	223	220	220	236	241	236	220	220	220	236	241	239	222	223	222	237.5	241	238

Conclusions

In this paper six PWM approaches are employed for five-level MLI-fed motor drives, and the results were compared. The three five-level-inverters used are CHB, NPC and PUC, which use PD, POD, APOD, COPD, COPOD and COAPOD SPWM switching methods. The earlier sections have covered the concepts of CMV, BC, multi-level inverters, as well as the aforementioned switching techniques. The last portion has covered the simulation results for the models that have been provided. According to the simulation results, a five-level multilevel inverter produces less CMV when using (POD) multicarrier PWM when modulation index is equal to 1 and in under modulation condition. In addition, based on the obtained results, when compared to other modulation approaches, PD modulation offers a better spectrum performance, lower Line voltage THD, and phase current THD. Moreover, the PUC inverter and COAPOD technique yield the finest simulation outcomes from the bearing current's point of view.

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