An Asymmetric Multi-Level Inverter Structure with Increased Steps per Devices

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***Abstract*—This paper suggests an improved basic single-phase 35-level inverter unit that consists of 4 DC power supplies, 4 capacitors, 10 switch/diodes and 10 gate driver circuits. The basic unit employs two DC links constructed by two cascaded capacitors in parallel with V_L and V_R DC sources. The use of capacitors not only has led to increased levels, but also has reduced the DC sources and converter cost. The voltage balancing of capacitors is done naturally which eases the control of proposed topology. Since, the proposed structure is based on developed H-bridge, it can produce positive, zero and negative voltage steps. Also, the suggested topology has suitable performance for resistive (*R*) or resistive-inductive (*R-L*) load types. Based on comparison results, the suggested structure has more steps per devices than similar configurations. The credits of suggested topology have been certified by comparisons and simulations in PSCAD/EMTDC software.**

Keywords— blocking voltage, capacitor based multi-level inverter, number of steps/devices

I. Introduction

The outstanding properties of Multi-Level Inverters (MLIs) have gained considerable popularity in research and industrial centers [1]. The MLIs generally benefit from simple and modular structure, expandability, suitability for medium/high voltage/power utilities, increased levels, low Total Harmonic Distortion (THD), improved quality and so on [2-4]. But, the MLIs require many devices (such as DC supplies and power semiconductors) to reach more levels, which leads to increased volume and cost [5]. Many reduced device oriented MLI structures have been presented in literature [6-10]. But, the DC supplies are the bulkiest, heaviest and most expensive parts of MLIs. So, the main objective is to replace them with cheaper, smaller and lighter energy sources such as capacitors [11-13]. Utilization of capacitors in MLIs can lead to reduced DC sources and/or increased gain [14-19]. The charge (or voltage) balancing is the main challenge of Capacitor Based MLIs (CBMLIs) [20]. The voltage balancing of capacitors of MLIs can be realized naturally or through additional circuits, which increase the size and complicates control of converter [17, 21]. This study examines only unity gain CBMLIs.

The CBMLIs presented in [22-27] have unity gain and use capacitors to reduce DC source count. The CBMLIs presented in [22, 26, 27] apply developed H-Bridge unit for generating negative steps, where [24] employs conventional H-Bridge unit. Since each basic unit of [24] applies an H-Bridge, numerous switches are required at cascaded versions. The [22, 27] utilize numerous bidirectional switches and accordingly numerous MOSFETs to achieve increased levels. Also, the charge balancing of capacitors in 3 or more cascaded capacitor versions of [22, 27] is very difficult that demands an extra control strategy.

This paper proposes a developed CBMLI topology with enhanced levels per devices that leads to less THD, better quality, less size and expense. Also, the charge balance of capacitors are done naturally, which simplifies the control strategy. In the following sections, the suggested basic topology and extended versions are discussed. Then, comparison and simulation results are given. Finally, the conclusions are presented.

II. Suggested Basic Configuration

A. Configuration

As shown in Fig. 1, the suggested topology is consisted of 4 DC supplies, 4 capacitors and 10 power switches (6 unidirectional and 4 bidirectional). Each switch demands a driver circuit, so the count of switches and driver circuits are the same.

$$N_{Source} = N_{Capacitor} = 4, N_{Switch} = N_{Driver} = 10 \quad (1)$$

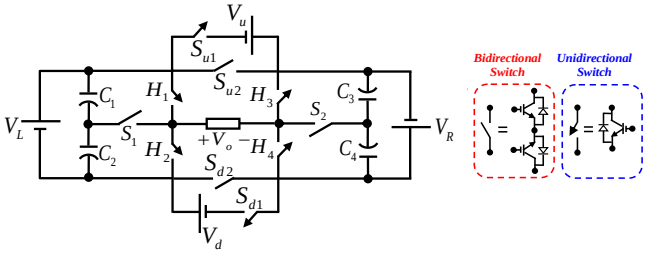


Fig. 1. Suggested basic topology.

B. Determination on Size of Power Supplies

To prevent generation of redundant levels and maximize distinct voltage steps, the size of DC supplies in suggested topology are selected as (2). Therefore, the variety of DC supplies is 3.

$$V_u = V_d = V_{dc}, V_R = 4V_{dc}, V_L = 12V_{dc} \quad (2)$$

C. Voltage on Capacitors

The (C_1, C_2) and also (C_3, C_4) are selected the same. The cascaded (C_1, C_2) and (C_3, C_4) have been connected in parallel with V_L and V_R, respectively. Accordingly, the voltage of C_1, C_2, C_3 and C_4 capacitors are naturally regulated on (V_L/2), (V_L/2), (V_R/2) and (V_R/2), respectively, as (3).

$$V_{C_1} = V_{C_2} = (V_L / 2) = 6V_{dc}, V_{C_3} = V_{C_4} = (V_R / 2) = 2V_{dc} \quad (3)$$

D. Switching States

The switching states of suggested basic configuration have been shown in Table I. It is seen that the suggested basic unit can create 17 positive, 17 negative and zero voltage steps.

TABLE I. SWITCHING STATES OF SUGGESTED BASIC TOPOLOGY

No.	S_1	S_2	S_{u1}	S_{u2}	S_{d1}	S_{d2}	H_1	H_2	H_3	H_4	V_o	
1	0	0	0	1	0	0	1	0	1	0	0	0
	0	0	0	0	0	1	0	1	0	1		
2	0	0	0	0	1	0	0	1	0	1	$+V_{dc}$	$+V_d$
3	0	0	1	0	0	0	1	0	1	0	$-V_{dc}$	$-V_u$
4	0	1	0	0	0	1	0	1	0	0	$+2V_{dc}$	$+V_R/2$
5	0	1	0	1	0	0	1	0	0	0	$-2V_{dc}$	$-V_R/2$
6	0	1	0	0	1	0	0	1	0	0	$+3V_{dc}$	$V_d+V_R/2$
7	0	1	1	0	0	0	1	0	0	0	$-3V_{dc}$	$-V_u-V_R/2$
8	0	0	0	0	0	1	0	1	1	0	$+4V_{dc}$	$+V_R$
9	0	0	0	1	0	0	1	0	0	1	$-4V_{dc}$	$-V_R$
10	0	0	0	0	1	0	0	1	1	0	$+5V_{dc}$	$+V_d+V_R$
11	0	0	1	0	0	0	1	0	0	1	$-5V_{dc}$	$-V_u-V_R$
12	1	0	0	0	0	1	0	0	0	1	$+6V_{dc}$	$+V_L/2$
13	1	0	0	1	0	0	0	0	1	0	$-6V_{dc}$	$-V_L/2$
14	1	0	0	0	1	0	0	0	0	1	$+7V_{dc}$	$V_d+(V_L/2)$
15	1	0	1	0	0	0	0	0	1	0	$-7V_{dc}$	$-V_u-(V_L/2)$
16	1	1	0	0	0	1	0	0	0	0	$+8V_{dc}$	$(V_L+V_R)/2$
17	1	1	0	1	0	0	0	0	0	0	$-8V_{dc}$	$-(V_L+V_R)/2$
18	1	1	0	0	1	0	0	0	0	0	$+9V_{dc}$	$(V_L+V_R)/2+V_d$
19	1	1	1	0	0	0	0	0	0	0	$-9V_{dc}$	$-(V_L+V_R)/2-V_u$
20	1	0	0	0	0	1	0	0	1	0	$+10V_{dc}$	$V_R+(V_L/2)$
21	1	0	0	1	0	0	0	0	0	1	$-10V_{dc}$	$-V_R-(V_L/2)$
22	1	0	0	0	1	0	0	0	1	0	$+11V_{dc}$	$V_R+(V_L/2)+V_d$
23	1	0	1	0	0	0	0	0	0	1	$-11V_{dc}$	$-V_R-(V_L/2)-V_u$
24	0	0	0	0	0	1	1	0	0	1	$+12V_{dc}$	$+V_L$
25	0	0	0	1	0	0	0	1	1	0	$-12V_{dc}$	$-V_L$
26	0	0	0	0	1	0	1	0	0	1	$+13V_{dc}$	$+V_L+V_d$
27	0	0	1	0	0	0	0	1	1	0	$-13V_{dc}$	$-V_L-V_u$
28	0	1	0	0	0	1	1	0	0	0	$+14V_{dc}$	$+V_L+(V_R/2)$
29	0	1	0	1	0	0	0	1	0	0	$-14V_{dc}$	$-V_L-(V_R/2)$
30	0	1	0	0	1	0	1	0	0	0	$+15V_{dc}$	$V_L+(V_R/2)+V_d$
31	0	1	1	0	0	0	0	1	0	0	$-15V_{dc}$	$-V_L-(V_R/2)-V_u$
32	0	0	0	0	0	1	1	0	1	0	$+16V_{dc}$	V_L+V_R
33	0	0	0	1	0	0	0	1	0	1	$-16V_{dc}$	$-V_L-V_R$
34	0	0	0	0	1	0	1	0	1	0	$+17V_{dc}$	$V_L+V_d+V_R$
35	0	0	1	0	0	0	0	1	0	1	$-17V_{dc}$	$-V_L-V_u-V_R$

Maximum producible voltage of suggested basic topology is $V_{o,max}=17V_{dc}$, which is sum of V_L, V_R and V_u (or V_d). The number of steps of suggested basic unit can be computed as:

$$N_{Step}=2(V_{o,\max}/V_{dc})+1=35 \quad (4)$$

E. Blocking Voltage on Switches

Blocking Voltage (BV), Normalized Blocking Voltage (NBV) and Average of NBVs (ANBV) on switches of suggested basic converter have been shown Table II.

TABLE II. BLOCKING VOLTAGE ON SWITCHES OF PROPOSED TOPOLOGY

Switch	*BV*	*NBV* [%]	*Switch*	*BV*	*NBV* [%]
S_1	$V_L/2=6V_{dc}$	35.3	S_{d2}	$V_L+V_u+V_R=17V_{dc}$	100
S_2	$V_R/2=2V_{dc}$	11.76	H_1	$V_L=12V_{dc}$	70.58
S_{u1}	$V_L+2V_u+V_R=18V_{dc}$	105	H_2	$V_L=12V_{dc}$	70.58
S_{u2}	$V_L+V_u+V_R=17V_{dc}$	100	H_3	$V_R=4V_{dc}$	23.53
S_{d1}	$V_L+2V_u+V_R=18V_{dc}$	105	H_4	$V_R=4V_{dc}$	23.53
Average of BVs= $\frac{\sum BV_{S,T}}{N_{switch}}$ **=11V_{dc}**			**Average of NBVs=** $\frac{\sum BV_{S,T}}{N_{switch}\times V_{o,\max}}$ =64.706 [%]		

It is observed that the (S_{u1}, S_{d1}) are imposed to $18V_{dc}$, which is 5[%] more than $V_{o,max}$. Also, the BV of (S_{u2}, S_{d2}) are equal to $V_{o,max}=17V_{dc}$. The BV on other switches are less than $V_{o,max}$. The high BV on (S_{u1}, S_{d1}) is the main drawback of proposed topology.

III. SUGGESTED EXTENDED TOPOLOGIES

A. First Extended topology (P_1)

As seen from Fig. 2, the suggested basic structure can be extended by increment of cascaded capacitors in right and left DC links, which increases number of steps, while keeping the number of DC supplies the same. The device count of 1st extended topology is calculated from (5):

$$N_{Source}=4, N_{Switch}=N_{Driver}=2n+6, N_{Capacitor}=2n \quad (5)$$

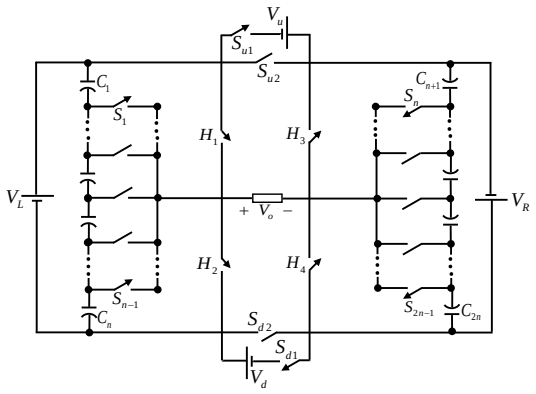


Fig. 2. Proposed 1st extended topology (P_1)

To create maximum number of steps, the amplitude of DC sources should be selected as (6). Thus, the variety of DC sources is $N_{Variety}=3$.

$$V_u=V_d=V_{dc}, V_R=2nV_{dc}, V_L=2n(n+1)V_{dc} \quad (6)$$

Where, n shows the number of cascaded capacitors in each DC link. In such arrangement, the voltage of capacitors will be regulated on values presented in (7):

$$V_{C_{L,i}}=(V_L/n)=2(n+1)V_{dc}, V_{C_{R,i}}=(V_R/n)=2V_{dc} \quad (7)$$

The peak output voltage and also number of steps of proposed 1st extended topology can be computed respectively from (8)-(9).

$$V_{o,\max}=(2n^2+4n+1)V_{dc} \quad (8)$$

$$N_{Step}=4n^2+8n+3 \quad (9)$$

B. Second Extended topology (P_2)

The proposed 2nd extended structure is made by cascading basic units, as shown in Fig. 3. The number of required devices are as (10), where, n denotes number of cascaded units. The count of required unidirectional and bidirectional switches are respectively $2n$ and $8n$.

$$N_{Source}=N_{Capacitor}=4n, N_{Switch}=N_{Driver}=10n \quad (10)$$

The size of DC supplies should be chosen as (11) to produce maximum steps, where i=1, 2, ⋯, n.

$$V_{L,i}=12(18)^{i-1}V_{dc}, V_{R,i}=4(18)^{i-1}V_{dc}$$
$$V_{u,i}=V_{d,i}=(18)^{i-1}V_{dc} \quad (11)$$

Based on (11), the variety of DC sources, maximum output voltage and number of steps of proposed 2nd extended configuration can be calculated from (12)-(14), respectively.

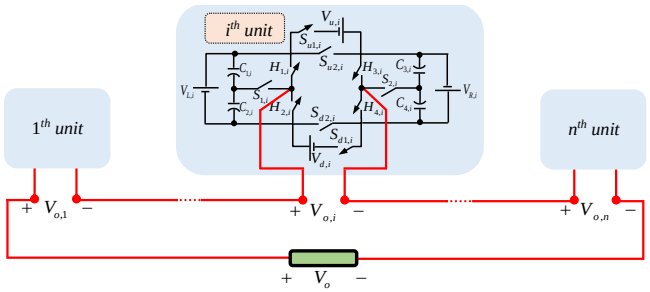


Fig. 3. Proposed 2nd extended topology (P_2)

$$N_{Variety} = 3n \tag{12}$$

$$V_{o,\max} = (18^n - 1)V_{dc} \tag{13}$$

$$N_{Step} = 2(18)^n - 1 \tag{14}$$

IV. Comparison Results

In this part, different features of suggested topology are contrasted with that of similar structures presented in [23, 24] and [25-27]. The results have been summarized in Table III and graphically shown in Fig. 4.

TABLE III. Comparison Results

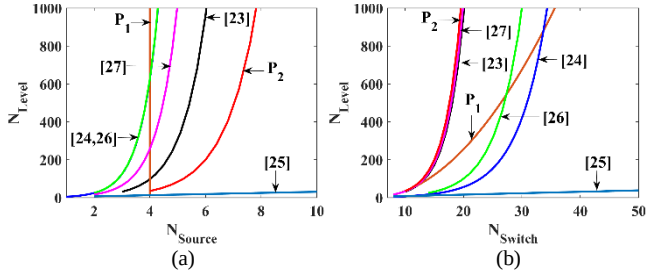
Topology	[23]	[24]	[25]	[26]	[27]	P_1	P_2
N_{Level}	31^n	5^n	$6n+1$	25^n	16^n+1	$4n^2+8n+3$	34^n+1
ANVs[%]	51.5	75	64.3	51.67	81.25	64.7	64.7
$N_{Variety}$	$2n$	n	$2n$	$2n$	$2n$	3	$3n$
$V_{o,max}/V_{dc}$	$(31^n-1)/2$	$(5^n-1)/2$	$3n$	$(25^n-1)/2$	$16^n/2$	$2n^2+4n+1$	$34^n/2$
N_{Source}	$3n$	n	$2n$	$2n$	$2n$	4	$4n$
N_{Switch}	$10n$	$8n$	$8n$	$14n$	$8n$	$2n+6$	$10n$
$N_{Capacitor}$	$5n$	$2n$	$2n$	$4n$	$4n$	$2n$	$4n$
$N_{Component}$	$28n$	$19n$	$19n$	$34n$	$22n$	$6n+16$	$28n$
N_{Driver}	$10n$	$8n$	$7n$	$14n$	$8n$	$2n+6$	$10n$

According to Fig. 4a, the proposed 1st extended topology (P_1) can produce increased steps by only 4 DC sources, but at low/medium number of steps, the [24] and [26] produce higher N_{Level}/N_{Source} than others.

Figs. 4b-4d validates that the suggested 2nd extended topology (P_2) can produced more steps than other topologies by using the same switches/driver-circuits/components. This can lead to a reduction in volume, expense, loss and complexity of converter.

Fig. 4e shows that at medium/high levels, the variety of DC sources of P_1 remains constant on 4, but the other structures require higher varieties, which can lead to increased cost.

It is seen from Fig. 4f that by using the same capacitor count, the P_2 can produce more steps than other configurations. Also with the same count of devices, the P_2 and [27] can produce larger peak output voltages ($V_{o,max}$) than others, leading to higher output powers.



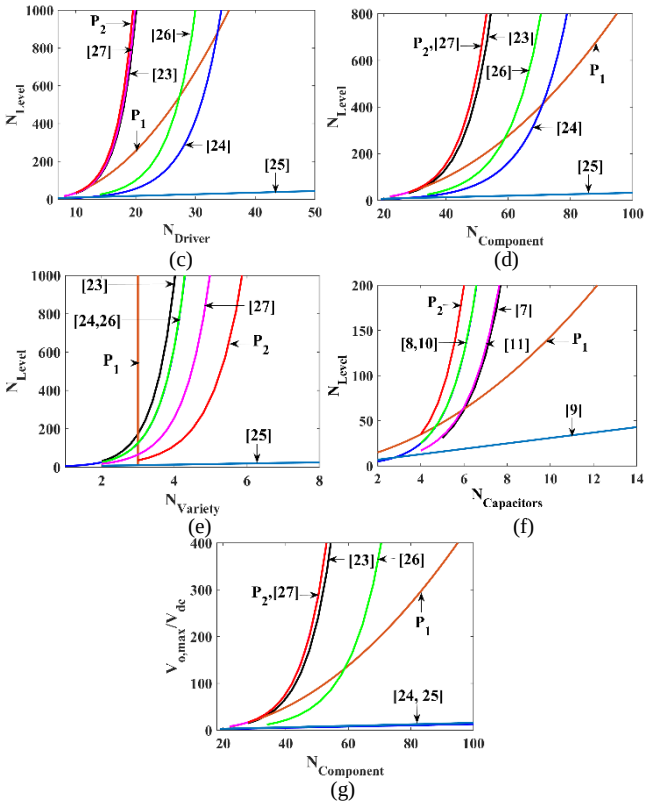


Fig. 4. Comparison results a) N_{Level} vs. N_{Source}, b) N_{Level} vs. N_{Switch}, c) N_{Level} vs. N_{Driver}, d) N_{Level} vs. $N_{Component}$, e) N_{Level} vs. $N_{Variety}$, f) N_{Level} vs. $N_{Capacitor}$, g) $V_{o,max}$ vs. $N_{Component}$.

V. Simulation Results

The suggested basic unit is simulated in PSCAD/EMTDC software to assure of its appropriate performance. The simulation parameters have been listed in Table IV. The fundamental frequency methodology has been employed for generation switching pulses.

TABLE IV. Simulation Parameters

Parameter	Value
Fundamental frequency (f)	50[Hz]
Modulation index (m)	1
DC sources (V_L,V_R,V_u,V_d)	V_L=120[V], V_R=40[V],V_u=V_d=10[V]
Load (R-L)	R=170[Ω], L=200[mH]

Fig. 5 indicates that the suggested basic topology has efficiently produced 35 steps (0, ±10, ±20, ⋯, ±170) with maximum output voltage of $V_{o,max}$=170[V]. The load current magnitude is about $I_{o,max}$≈0.94[A].

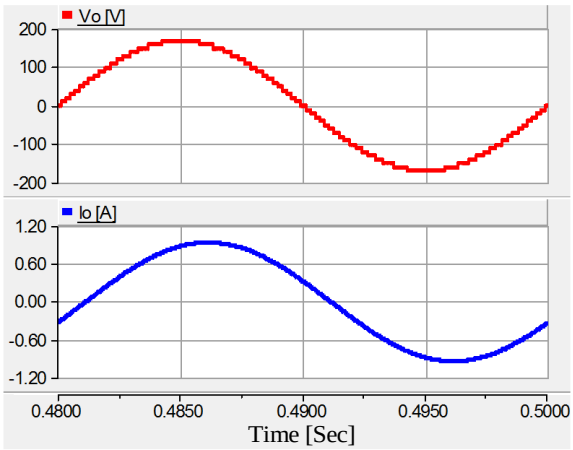


Fig. 5. Load voltage and current waveforms.

The phase difference of $\Delta\varphi \approx 20^{\circ}$ (validated by (12)) between load voltage and current waveforms confirms suitability of suggested topology for supplying *R-L* load types.

$$\arctan(L\omega / R) \approx 20^{\circ} \quad (12)$$

The THD of output voltage is about 2.12[%]. Due to small THD, the output filter can be removed or downsized, leading to reduced volume and expense of converter. The harmonic spectrum of output voltage of suggested configuration has been depicted in Fig. 6. It is seen that the magnitude of fundamental frequency order is 100[%], where the magnitude of other harmonic orders are much less than 0.5[%].

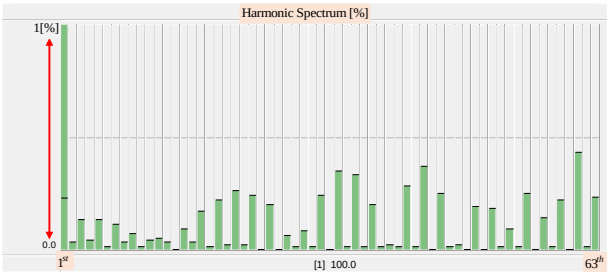


Fig. 6. Harmonic spectrum of output voltage waveforms.

The voltage waveform of switches have been shown in Fig. 7. This figure indicates that the *BV* on switches are about BV_{S1}=60[*V*], BV_{S2}=20[*V*], BV_{Su1}=180[*V*], BV_{Su2}=170[*V*], BV_{Sd1}=180[*V*], BV_{Sd2}=170[*V*], BV_{H1}=120[*V*], BV_{H2}=120[*V*], BV_{H3}=40[*V*], BV_{H4}=40[*V*], which are verified by Table II.

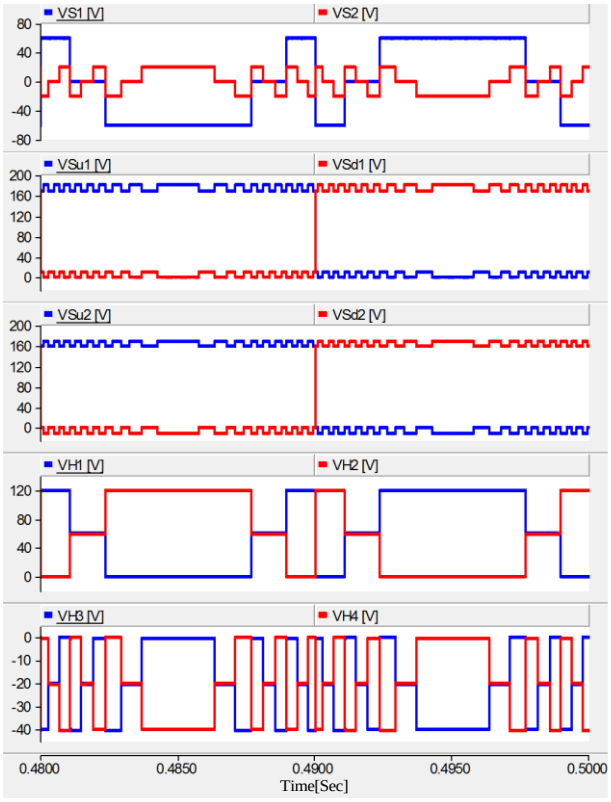


Fig. 7. Voltage waveform on switches.

The current waveform of switches have also been shown in Fig. 8. The current stress of switches are as follow: I_{S1}=I_{S2}=0.94[*A*], I_{Su1}=I_{Su2}=0.94[*A*], I_{Sd1}=I_{Sd2}=0.94[*A*], I_{H1}=I_{H2}=0.94[*A*], I_{H3}=I_{H4}=0.94[*A*]. Since the load current flows through the switches, the current stress of all switches is equal to the load current amplitude, which is $I_{o,max}$=0.94[*A*].

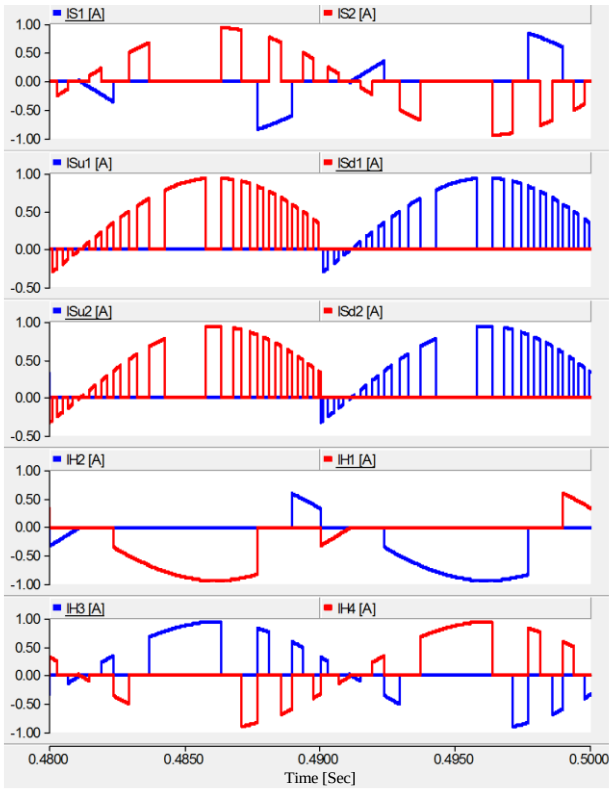


Fig. 8. Current waveforms of switches.

VI. Conclusions

This paper has proposed a basic capacitor-based 35-level inverter topology that can be extended either by increasing the cascaded capacitors of right and left DC-links or by cascading of basic unit. Application of capacitors has led to less DC supplies and consequently less volume and cost. The proposed basic and extended topologies have larger ratio of steps per switches, driver circuits, capacitors and total components than other similar structures. This means that by the same count of devices, the proposed topologies can produce more steps than others. Also, it is observed that for generating the same levels, the proposed topologies utilize less switches, driver circuits, capacitors and total devices than other topologies, which leads to reduced size and expense of converter. The proposed 1st extended structure can produce increased levels only by 4 DC supplies. Low THD, downsized output filter, natural voltage balancing of capacitors as well as capability of supplying *R-L* loads are other merits of proposed topologies, while the high blocking voltage on S_{u1} and S_{d1} is the main drawback. The claimed advantages and correct performance of proposed topologies have been confirmed by comparison and simulations results.

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