A Boost Switched-Capacitor Multilevel Inverter with Self-Balance and Inductive-load Ability

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***Abstract*— This article presents a single phase eleven-level inverter based on switched-capacitor (SC) technique, which can realize eleven-level output with single dc source. In addition, it can produce more levels by a cascaded structure. Without utilizing the auxiliary balance circuits, or complicated control strategies, the two capacitors in series connection can innately keep voltage balance at $0.5V_{dc}$, and the floating capacitor can obtain self-balance at V_{dc}. The merits of the eleven-level switched-capacitor inverter (11-LSCI) on reduced components, capacitors self-balance capability, enhance output amplitude and inductive-load ability are also illustrated through the comparison against other proposed multilevel inverters (MLIs). It should be noted that less semiconductor components in the proposed topology reduce switching and conduction losses. Therefore, increases efficiency. Finally, the simulation results are brought to verify the effectiveness and performance of the presented inverter.**

Keywords*— multilevel, switched-capacitor, self-balance, voltage boost, inductive-load ability.

I. INTRODUCTION

In recent years, multilevel inverters have been widely utilized in electrical power distribution system, renewable energy generation (REG) [1], industrial applications and transportation [2]. Because of the merits like generate more levels in the output, quasi-sinusoidal output waveform, lower switching frequency, higher efficiency, less Total Harmonic Distortion (THD), improved electromagnetic interference (EMI) and so on [3], the research and development continues in this field and various topologies are introduced by researchers each year.

Classical MLIs are divided into three types: neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) topologies. NPC and FC both suffer the restrictions such as voltage unbalance of capacitors, the numerous semiconductor components and capacitors, particularly when the output level increases more than seven. On the other hand, it's true that CHB can attain a significant output level with fewer power switches. However, it needs several isolated dc power supplies at higher levels [4].

To overcome these drawbacks in traditional MLIs, many efforts have been done and many techniques have also been presented. For instance, the transformer-based inverters [5] or quasi z-source inverters [6]. The switched-capacitor (SC) technique has also been extensively investigated as a novel approach to work out aforesaid problems and it has attracted a lot of attention in academia and industry. The SC MLIs with reduced power devices and voltage boost ability were proposed in [7] and [8]. In SC inverters, there is no need for ancillary equilibrium circuits, current and voltage sensors or complex control algorithms, since the voltage of each capacitor can be automatically balanced in a cycle. Another benefit of SC MLIs is the ability to boost output voltage.

It is worth noting that the presented inverter in this article is also a SC MLI. The significant advantages of the proposed topology are included the decreased devices, capacitors self-balance capability, 2.5 voltage gain and inductive-load ability. Also, the presented inverter can produces more output levels through cascaded structure with the same parameters design.

Following this section, the circuit configuration, the operation modes at different levels and self-voltage balancing method of the capacitors are described in detail as well. The modulation strategy, capacitance calculation and the loss evaluation are given in Section III. The comparison of the proposed inverter against other topologies is carried out in Section IV based on reduced components, dv/dt stress and total cost. The extended structure is also introduced. In Section V, the simulation results validate performance of the proposed 11-level topology. Lastly, the conclusions are given in Section VI.

II. PROPOSED 11-LEVEL SC INVERTER

A. Circuit Description

The basic idea of the proposed topology is originated from [7] and [9]. The circuit configuration of the 11-LSCI is shown in Fig.1. It includes a single dc input, three switched capacitors C_1 to C_3, a power diode D and ten active switches, in which S_5 and S_6 are bidirectional switches. To achieve eleven-level output ($\pm 2.5V_{dc}$, $\pm 2V_{dc}$, $\pm 1.5V_{dc}$, $\pm V_{dc}$, $\pm 0.5V_{dc}$,0) as well as boost voltage output, the capacitors C_1 to C_3 must be charged in parallel and discharged in series with the dc voltage source.

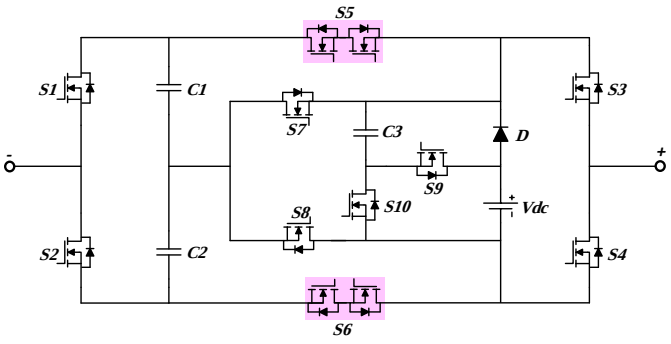

Fig. 1. Circuit configuration of the proposed inverter

B. Operating Cycles

The switching states of power MOSFETs and modes of the capacitors are summarized in Table I, where '1' indicates the switch is ON and '0' indicates the switch is OFF. As it

can be seen, the switch pairs (S_1, S_2), (S_3, S_4) and (S_9, S_{10}) are complementary switches, as well as 'C', 'D' and '-' denote the capacitors is charged, discharged and have not changed, respectively. The series capacitors C_1/C_2 and the capacitor C_3 are charged several times in one cycle and their voltages without any auxiliary balance circuits or complicated control strategy, naturally maintain at $0.5V_{dc}$ and V_{dc}, respectively. Meanwhile, the proposed inverter is capable to conduct the power flow in two ways. In Fig. 2, two conductive paths is shown. The red flow loops are current paths for resistive load and the blue flow loops are reverse current paths for inductive load. The green loops also indicate the charging paths of the capacitors.

Level $V_{Out} = 0$

As shown in Fig.2 (a), to achieve ***0*** output level, the S_2, S_4, S_5, S_6 and S_{10} switches are **ON** state while other switches are **OFF**. All three capacitors are charged in parallel connection with the input source.

Level $V_{Out} = 0.5V_{dc}$

As shown in Fig.2 (b), to achieve $+0.5V_{dc}$ output level, the S_2, S_4, S_8 and S_{10} switches are **ON** state while other switches are **OFF**. The capacitor C_2 is discharged to provide the load. The capacitor C_1 remains unchanged and C_3 is charged in parallel with the dc voltage source.

Level $V_{Out} = V_{dc}$

As shown in Fig.2 (c), to achieve $+V_{dc}$ output level, the S_2, S_3, S_5, S_6 and S_{10} switches are **ON** state while other switches are **OFF**. Output voltage is directly provided by the dc source. All three capacitors are charged in parallel connection with the input source.

Level $V_{Out} = 1.5V_{dc}$

As shown in Fig.2 (d), to achieve $+1.5V_{dc}$ output level, the S_2, S_3, S_8 and S_{10} switches are **ON** state while other switches are **OFF**. The load's needed energy is provided by the series connection of C_2 and the dc voltage source. The capacitor C_1 remains unchanged and C_3 is charged in parallel with the input source.

Level $V_{Out} = 2V_{dc}$

As shown in Fig.2 (e), to achieve $+2V_{dc}$ output level, the S_2, S_3, S_6 and S_9 switches are **ON** state while other switches are **OFF**. The load's needed energy is provided by the series connection of C_3 and the dc voltage source. The capacitors C_1 and C_2 remain unchanged.

Level $V_{Out} = 2.5V_{dc}$

As shown in Fig.2 (f), to achieve $+2.5V_{dc}$ output level, the S_2, S_3, S_8 and S_9 switches are **ON** state while other switches are **OFF**. The load's needed energy is provided by the series connection of C_2, C_3 and the dc voltage source. The capacitor C_1 remains unchanged.

Level $V_{Out} = -0.5V_{dc}$

As shown in Fig.2 (g), to achieve $-0.5V_{dc}$ output level, the S_1, S_3, S_7 and S_{10} switches are **ON** state while other switches are **OFF**. The capacitor C_1 is discharged to provide the load. The capacitor C_2 remains unchanged and C_3 is charged in parallel with the dc voltage source.

Level $V_{Out} = -V_{dc}$

As shown in Fig.2 (h), to achieve $-V_{dc}$ output level, the S_1, S_4, S_5, S_6 and S_{10} switches are **ON** state while other switches are **OFF**. Output voltage is directly provided by the dc source. All three capacitors are charged in parallel connection with the input source.

Level $V_{Out} = -1.5V_{dc}$

As shown in Fig.2 (i), to achieve $-1.5V_{dc}$ output level, the S_1, S_4, S_7 and S_{10} switches are **ON** state while other switches are **OFF**. The load's needed energy is provided by the series connection of C_1 and the dc voltage source. The capacitor C_2 remains unchanged and C_3 is charged in parallel with the input source.

Level $V_{Out} = -2V_{dc}$

As shown in Fig.2 (j), to achieve $-2V_{dc}$ output level, the S_1, S_4, S_5 and S_9 switches are **ON** state while other switches are **OFF**. The load's needed energy is provided by the series connection of C_3 and the dc voltage source. The capacitors C_1 and C_2 remain unchanged.

Level $V_{Out} = -2.5V_{dc}$

As shown in Fig.2 (k), to achieve $-2.5V_{dc}$ output level, the S_1, S_4, S_7 and S_9 switches are **ON** state while other switches are **OFF**. The load's needed energy is provided by the series connection of C_1, C_3 and the dc voltage source. The capacitor C_2 remains unchanged.

TABLE I.
SWITCHING AND CAPACITOR STATES OF THE PRESENTED 11-LSCI

Output levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	C_1	C_2	C_3
$+2.5V_{dc}$	0	1	1	0	0	0	0	1	1	0	-	D	D
$+2V_{dc}$	0	1	1	0	0	1	0	0	1	0	-	-	D
$+1.5V_{dc}$	0	1	1	0	0	0	0	1	0	1	-	D	C
$+V_{dc}$	0	1	1	0	1	1	0	0	0	1	C	C	C
$+0.5V_{dc}$	0	1	0	1	0	0	0	1	0	1	-	D	C
0	0	1	0	1	1	1	0	0	0	1	C	C	C
0	1	0	1	0	1	1	0	0	0	1	C	C	C
$-0.5V_{dc}$	1	0	1	0	0	0	1	0	0	1	D	-	C
$-V_{dc}$	1	0	0	1	1	1	0	0	0	1	C	C	C
$-1.5V_{dc}$	1	0	0	1	0	0	1	0	0	1	D	-	C
$-2V_{dc}$	1	0	0	1	1	0	0	0	1	0	-	-	D
$-2.5V_{dc}$	1	0	0	1	0	0	1	0	1	0	D	-	D

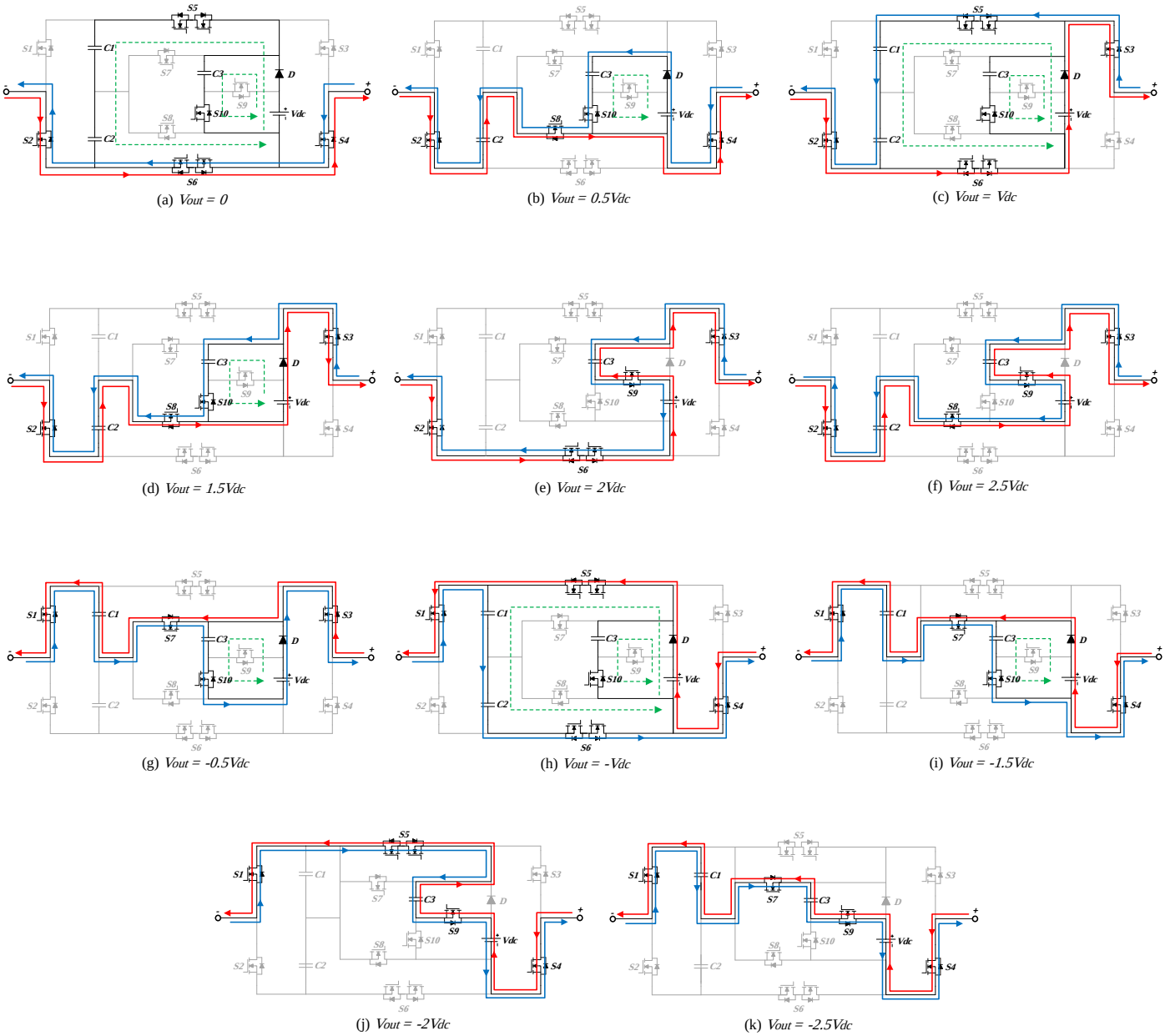

Fig. 2. The operational states and current flowing paths of the presented 11-LSCI at different output levels

III. Modulation Strategy, Capacitance Analysis and Calculation Of Power Losses

A. *Modulation Method for the proposed 11-LSCI*

A types of modulation methods can be used for MLIs, such as the phase disposition pulse width modulation (PD-PWM), selective harmonic elimination (SHE) PWM, third harmonic injection (THI) PWM and etc. In this paper, the PD-PWM is applied to reduce THD. As shown in Fig. 3, ten categories of triangle carriers, from top to bottom is V_{cri1} to V_{cri10}, with the same frequency, phase, and amplitude are compared with the sinusoidal waveform to generate the signal drives of switches. The carrier amplitude is V_c and the sinusoidal waveform amplitude is V_m. Therefore, the modulation index can be obtained:

$$M_a = \frac{V_m}{5V_c} \quad (1)$$

The modulation index depends on the number of output levels. For $0 < M_a \leq 1/5$, the proposed topology produces three output levels, which are $0.5V_{dc}$, 0, $-0.5V_{dc}$. For $1/5 < M_a \leq 2/5$, it generates five output levels that include V_{dc}, $0.5V_{dc}$, 0, $-0.5V_{dc}$, $-V_{dc}$. For $2/5 < M_a \leq 3/5$, it can synthesize seven output levels that comprise of $1.5V_{dc}$, V_{dc}, $0.5V_{dc}$, 0, $-0.5V_{dc}$, $-V_{dc}$, $-1.5V_{dc}$. For $3/5 < M_a \leq 4/5$, it produces nine output levels that comprise of $2V_{dc}$, $1.5V_{dc}$, V_{dc}, $0.5V_{dc}$, 0, $-0.5V_{dc}$, $-V_{dc}$, $-1.5V_{dc}$, $-2V_{dc}$. And to achieve the eleven-level staircase output, the modulation index must be greater than 4/5. Meanwhile, the presented circuit is able to work in over modulation condition.

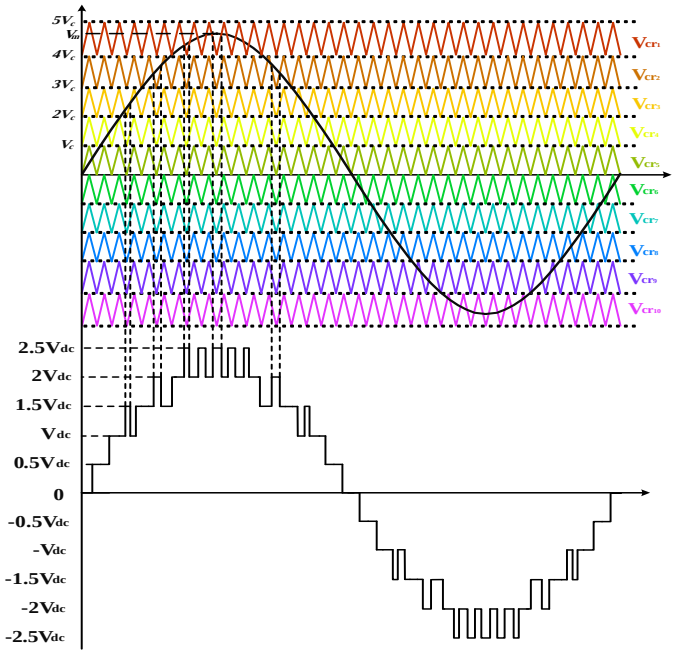

Fig. 3. The staircase output with fundamental frequency arising from the PD-PWM modulation

B. Capacitance Calculation

The maximum voltage ripple for each capacitor happens during the largest discharging time. Actually, during this time the saved energy in the capacitors is pumped to the load side, this situation is repeated in each cycle. Assuming that the load is pure resistor, the continuous discharging value of C_i during its largest discharging time [t_{ai}, t_{bi}] will be calculated as:

$$\Delta Q_i = \int_{t_{ai}}^{t_{bi}} \sqrt{2} I_L Sin(2\pi f_o t) dt \qquad (2)$$

Hence, the capacitance of C_i should be selected:

$$C_i > \frac{\Delta Q_i}{\Delta Vi} \qquad (3)$$

Where ΔV_i and I_L imply to the admissible voltage ripple for the capacitor C_i and the load current across it, respectively. The voltage ripple over capacitors should be less than 10% of the capacitor's maximum voltage. In the inductive loads, the capacitor's ripple voltage should be less than that in the pure resistor loads [10].

C. Analysis of power losses

To evaluate total power losses, three types of losses must be considered, as follows:

1) Switching Loss

Overlapping of the voltage and current of a switch leads to incidence of switching losses which occur during transition time from on-state to off-state or vice versa, where the switch is not fully turned on or off. The higher the switching frequency means the greater the number of times the switch changes state per second. Thus, these losses are proportional to the switching frequency and can be calculated as:

$$P_{sw} = \left(E_{on(S)} + E_{off(S)}\right) f_{sw} \qquad (4)$$

Where $E_{on(S)}$ and $E_{off(S)}$ are the switch turn-on and turn-off energy losses, and f_{sw} is the switching frequency.

2) Conduction Loss

The conduction losses are arising from the parasitic parameters in the output current paths, which are chiefly consists of the internal resistance of capacitors (r_c), the on-state resistance of the switches (r_s) and diodes (r_d). The higher the number of conducting devices in the load current path, means the much higher the conduction losses, and the lower efficiency. The total parasitic impedance for 11-LSCI is presented in Table II at each output level.

TABLE II.
TOTAL PARASITIC IMPEDANCE AT EACH OUTPUT LEVEL

Output levels	Total parasitic impedance
0	$3r_s$
$\pm 0.5V_{dc}$	$3r_s + r_c$
$\pm V_{dc}$	$3r_s + r_d$
$\pm 1.5V_{dc}$	$3r_s + r_d + r_c$
$\pm 2V_{dc}$	$4r_s + r_c$
$\pm 2.5V_{dc}$	$4r_s + 2r_c$

The conduction losses of the proposed inverter expressed as:

$$\begin{aligned} P_{con} &= P_{con(0)} + P_{con<0.5>} + P_{con<1>} + P_{con<1.5>} + P_{con<2>} + P_{con<2.5>} \\ P_{con} &= 4 f_o [I^2_{L<0>}(3r_s)T_{<0>} + I^2_{L<0.5>}(3r_s + r_c)T_{<0.5>} \\ &\quad + I^2_{L<1>}(3r_s + r_d)T_{<1>} + I^2_{L<1.5>}(3r_s + r_d + r_c)T_{<1.5>} \\ &\quad + I^2_{L<2>}(4r_s + r_c)T_{<2>} + I^2_{L<2.5>}(4r_s + 2r_c)T_{<2.5>}] \end{aligned} \qquad (5)$$

3) Ripple loss

The ripple losses occur due to the process of charging capacitors and can be calculated as:

$$P_{rip} = f_o C_i \Delta V_i^2 \qquad (6)$$

Where f_o is fundamental frequency, C_i and ΔV_i are capacitance and allowed voltage ripple for the i^{th} capacitor. In Fig. 4 the equivalent charging circuit of capacitors C_1, C_2 and C_3 is illustrated.

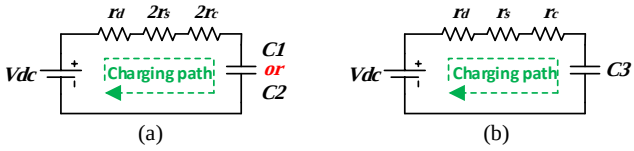

Fig. 4. The equivalent charging circuit at level $+V_{dc}$ for capacitors C_1/C_2 (a) capacitor C_3 (b)

Eventually, the total power losses are achieved by sum of the equations 4, 5 and 6.

$$P_{loss} = P_{sw} + P_{con} + P_{rip} \qquad (7)$$

IV. PERFORMANCE COMPARISONS AND EXTENSION

A. Quantitative Comparisons against other MLIs

In this part, comparisons are made between proposed inverter and other MLIs to highlight its pros and cons. The results are summarized in Table III, wherein 'N_{semi}' and 'N_{cap}' represent the number of semiconductor components (switches and diodes) and the number of capacitors, respectively. It is

expected that all the MLIs of under investigation utilize from single source to produce eleven output levels.

TABLE III.
COMPARISON RESULTS OF THE PROPOSED INVERTER AMONG OTHER MLIS

Comparable items	[11]	[12]	[13]	[14]	Proposed
N_{sem}	15	24	28	17	13
N_{cap}	3	4	5	5	3
Self-balance	Yes	Yes	Yes	Yes	Yes
Boost ability	Yes	Yes	Yes	No	Yes
TSV_{pu}	5.8	4.8	9.6	8.4	6.4
CF	20.9	30.4	37.8	26.2	19.2

It is obvious that the proposed 11-LSCI uses from fewer components for the same output levels compared with the other topologies. Hereby, the total power losses are reduced and consequently the efficiency in the proposed topology is increased.

The total standing voltage (TSV) describes the total voltage rating of the semiconductor components in a topology, and is calculated as:

$$TSV_{pu} = \frac{\sum_{i=1}^{n} V_{PIV\_SW_i} + \sum_{j=1}^{n} V_{PIV\_D_i}}{V_{o(\max)}} \qquad (8)$$

Where V_{PIV_SWi} and V_{PIV_Di} represent the peak inverse voltage (PIV) of each switch and diode in the circuit, respectively. $V_{o(max)}$ is the maximum amplitude of output voltage. From the aspect of TSV, the topologies in [11] and [12] have less TSV values than the proposed inverter but the other two circuits in [13] and [14] must be endure the much higher TSV.

To estimate the total cost of MLIs like article of [8], the cost function (CF) is discussed here.

$$CF = N_{sem} + N_{cap} + \alpha TSV_{pu} \qquad (9)$$

Where α is the weight factor of TSV and here it is set to 0.5, since the number of circuit components is more important. In terms of the CF as well, the proposed inverter is in acceptable condition against other topologies.

B. *Extended structure*

To get more output levels, the proposed inverter can be developed by the cascaded structure. As shown in Fig. 5, this configuration is proper for applications such as the photovoltaic system that use the isolated sources. Here, the symmetric state is considered, which an inverter with *n* cells composed of the *n* input sources, *12n* switches, *n* diodes and *3n* capacitors generates *10n+1* output levels.

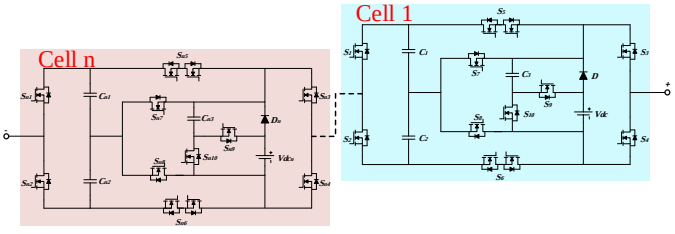

Fig. 5. The extended structure of proposed inverter

V. SIMULATION VERIFICATION

To approve the performance of the proposed 11-LSCI, its simulation is conducted on the MATLAB/Simulink. The simulation parameters are listed in Table IV.

TABLE IV.
THE CIRCUIT SIMULATION PARAMETERS

V_{dc}	f_o	f_{sw}	C_1/C_2	C_3	M_a
100V	50Hz	10kHz	2200μF	3600μF	0.9

Fig.6 (a) indicates waveforms of the output voltage V_o and current I_o with a pure load of *100Ω*. It can be understood that the output waveforms comprise from eleven stable levels and the maximum output voltage with the 100V input achieves to 250V, as a result, voltage boost ability for the proposed inverter is confirmed. Fig.6 (b) illustrates the harmonics spectrum of the output voltage. THD is 13.16%, and the fundamental voltage amplitude is 221.6V. Meanwhile, all of the harmonic orders are less than 0.35 percent. On the other hand, in Fig.6 (c) the inductive-load ability of the proposed topology for load of *100Ω-300mH* is verified. It can be observed that V_o is staircase waveform but I_o is sinusoidal for inductive loads. THD of output current is 0.11%.

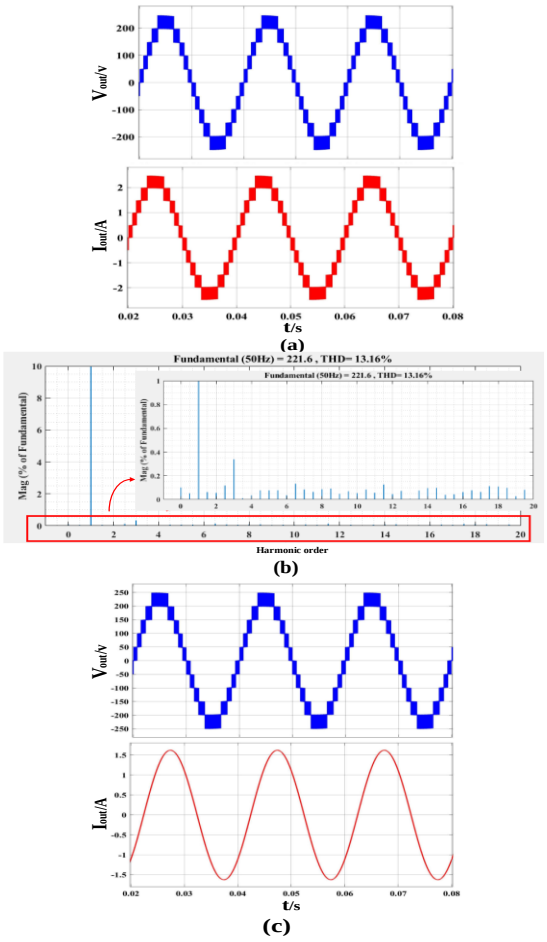

Fig. 6.Simulation results of the output voltage & current for pure load of *100Ω* (a) harmonic spectrum of output voltage (b) the output voltage & current for load of *100Ω-300mH* (c)

As shown in Fig.7 (a), all capacitors have maintained their expected voltage and their voltage ripple less than 3% is considered. This means that the capacitance of the capacitors can be selected less than the present value according to the equation (3). Fig.7 (b) shows the output voltage of the

topology due to a sudden change in the modulation index. As it can be seen that the voltage of all capacitors remain stable under various modulation index. Thus, capacitors self-balance capability is verified.

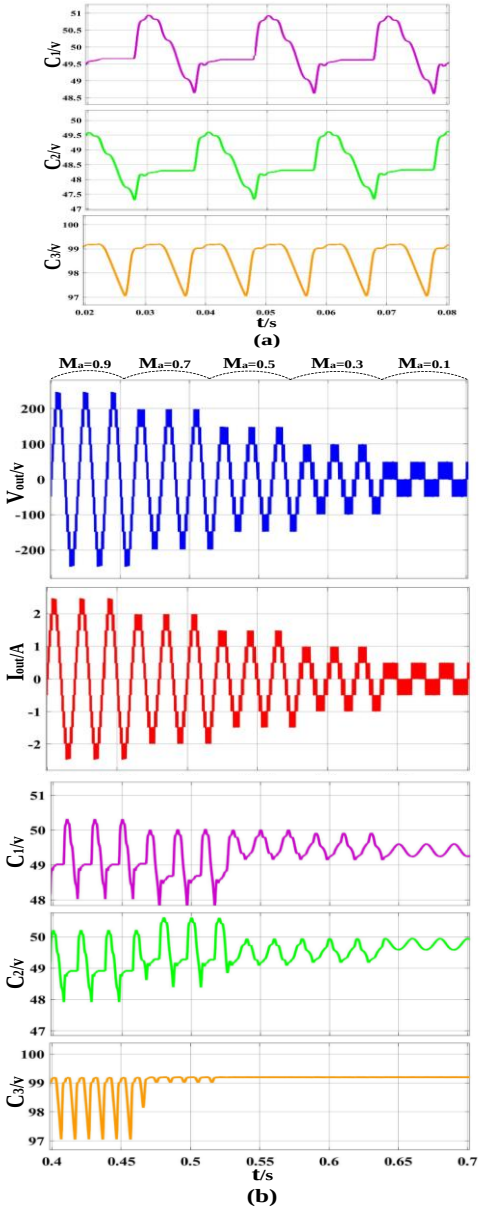

Fig. 7.Voltage of capacitors C_1, C_2 and C_3 for pure load of 100Ω (a) the output voltage, output current and voltage of capacitors when the modulation index varies from 0.9 to 0.1 (b)

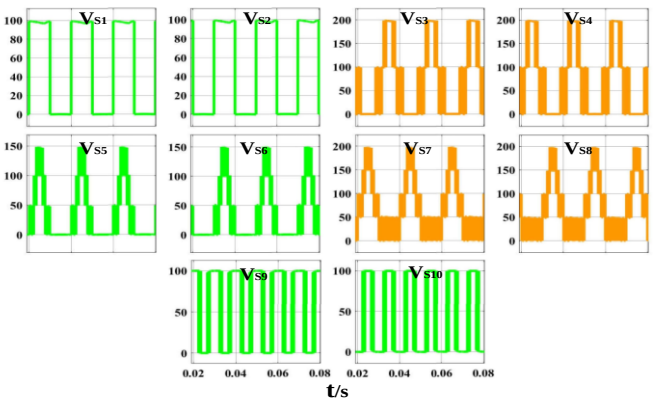

Fig. 8. Voltage stress of the switches S_1 - S_{10}

Fig.8 depicts the voltage stress of switches S_1-S_{10}. The PIV of switches S_3, S_4, S_7 and S_8 are double of the input source and the PIV of other switches do not exceed power supply amplitude.

VI. Conclusion

The eleven-level inverter based on switched-capacitor technique with reduced components, 2.5 voltage gain, self-balanced capacitors and inductive-load ability is presented in this paper. Also, the proposed inverter can generates more output levels through cascaded units with the same parameters design and this is an advantage for modular manufacturing and industrial applications. The circuit operation, capacitance analysis and loss evaluation is discussed in detail. Meanwhile, the comparison between proposed inverter with the existing circuits validates its advantages. Consequently, the simulation results prove the feasibility of the presented topology.

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