A New Reduced Switch Multilevel Inverter for PV Applications

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***Abstract*—According to the increase of Multi-Level Inverter (MLI) applications in distributed generations, a novel single-phase grid-connected MLI topology is proposed in this paper. The proposed inverter is intended to feed the utility grid from renewable energy sources (RESs) to overcome the problem of output sinusoidal waveform in conventional MLIs by generating a multilevel waveform with too many levels, and fewer switches count. The proposed structure is fault-tolerant and modular. A detailed analysis of the proposed topology for two different 13 and 20 switches have been carried out to show its superiority over the conventional MLI topologies. The 79-level and 321-level of the proposed MLI are designed and simulated in MATLAB/SIMULINK environment. After a precise simulation, due to compliance with the IEC 61727-2004, about total harmonic distortion (THD) of output voltage and current, there is no need to use extra output filter.**

Keywords—Multi-Level Inverter, Diode clamped inverter, flying capacitor inverter, Cascade H-bridge inverter, Topology, PV Application

I. INTRODUCTION

In recent years, electricity generation from renewable energy sources has grown tremendously. Likewise, with increasing power generation rates, the use of wind turbines, photovoltaic, and other renewable equipment has accelerated [1], [2]. Because the establishment and costs of renewable energy sources are still a bit expensive, the converters must be highly reliable and efficient to reduce the cost of return in addition to high performance [3]. Multilevel inverters have received much attention as a method of producing nearly sinusoidal waveforms by a large number of levels. As the number of levels increases, the number of power electronic switches and other circuit devices increases, so a topology with more levels and fewer switches are taken into consideration. Multilevel inverters have significant features such as improved output quality, better efficiency, fewer harmonics, and less switching stress on switches than conventional two-level inverters [4], [5]. Multilevel inverters have many advantages compared to two-level inverters such as lower switching losses, lower switching frequency, lower Common Mode voltage, higher efficiency, and better harmonic spectrum [6]. Multilevel inverters are an attractive solution in medium and high power applications [3]. They also show significant gains in reduced THD of power delivery for medium voltage sources [3]. MLIs are used in applications such as SVC and other FACTs, HVDC transmission lines, variable speed drive, and back-to-back systems [3], [7].

From the DC side point of view, MLIs are divided into two categories. The first is MLI with a common source such as Flying Capacitor (FC) MLI and Diode-Clamped (DC) MLI, and the second is MLI with isolated DC sources such as Cascade H-Bridge (CHB) MLI. These MLIs are used according to the type of application [8]. A large number of clamping diodes in DC-MLIs increases the cost and limits the use of high voltage applications [9]. As a result, most of the practical applications of the DC-MLIs are limited to less than five levels [10]. Also, in flying capacitor inverters, exceptional control is needed to balance capacitors voltages [11]. For PV applications with a large number of independent DC sources available, CHB-MLI is the preferred choice [12]. However, CHB-MLIs use a large number of switches, which results in more gate drive circuits and more complexity [13].

This paper presents a new MLI topology with fewer switches and also lower THD voltage than the other MLIs. Also, the proposed topology has modular capability and fault-tolerant. Circuit configuration and operation of the proposed MLI are discussed in section II. The simulation of 79-level and 321-level inverters are presented in section III. The comparison between the proposed MLI and conventional MLI is expressed in section IV.

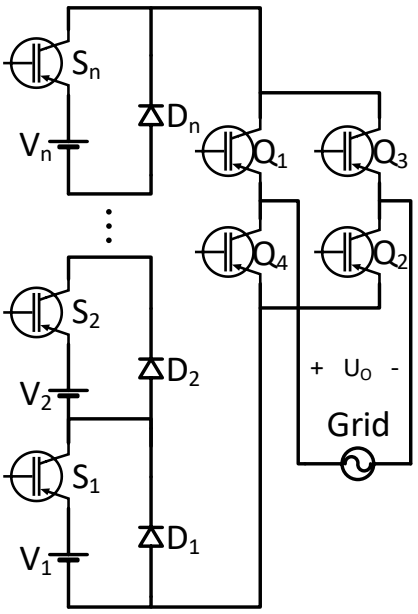
II. THE PROPOSED MLI TOPOLOGY

A. Circuit Configuration

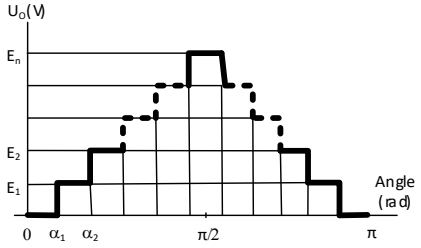
The proposed configuration consists of n independent DC sources, n switches, and n diodes, as shown in Fig. 1.a. In the proposed structure, both symmetric and asymmetrical DC sources can be employed. At the output of the configuration is an H-bridge inverter that allows alternating output levels of the proposed configuration. And just before the H-bridge is a structure for generating positive voltage levels.

B. Operation Principle

In this configuration, we have a switch for each independent DC voltage source. When each of these switches is turned on, the corresponding DC voltage source will be in series with the other independent DC sources, and its voltage is added to the voltage of the other series sources. The diodes with the corresponding switch, which is turned on, are reverse biased, and the diodes with the corresponding switch, which is turned off, are forward biased, thus closing the circuit. For the output voltage of the proposed topology, the U_1 to U_n voltages are generated for different switching modes.



(a)



(b)

Fig. 1. (a) Configuration of symmetric proposed MLI (b) Output waveform of the positive cycle

$$U_1 = V_1 \tag{1}$$

$$U_2 = V_1 + V_2 \tag{2}$$

$$U_n = V_1 + V_2 + \cdots + V_n \tag{3}$$

C. Operation in Symmetric Configuration

The proposed MLI with symmetric DC sources is composed of n independent and equal DC voltage sources. By turning on each switch, the value of V_{dc} is added to the output voltage of the converter, and by turning on the k switches, the output voltage will be kV_{dc}. Also, with n series independent DC voltage sources, each voltage level can be generated from 0 to nV_{dc} in the output. Likewise, by alternating the converter output voltage by H-bridge, the number of output levels of H-bridge inverter are 2n+1.

$$V_1 = V_2 = \cdots = V_n = V_{dc} \tag{4}$$

D. Operation in Asymmetrical Configuration

Different structures can be provided for this configuration with asymmetrical sources. We assume that the converter is made up of m number of the same modules in series, as shown in Fig. 2. Each module consists of n independent DC voltage sources, n switches, and n diodes. The voltage of these sources is V_1 to V_n. The voltage of these sources is three times the voltage V_1. So:

$$V_{i1} = \frac{1}{3}V_{i2} = \frac{1}{9}V_{i3} = \cdots = (\frac{1}{3})^{n-1}V_{in} = V_{dc} \tag{5}$$

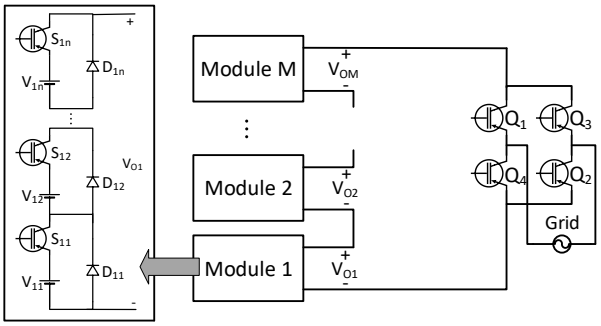


Fig. 2. Configuration of proposed Asymmetrical MLI

$$V_{i1} = \frac{1}{3}V_{i2} = \frac{1}{9}V_{i3} = \cdots = (\frac{1}{3})^{n-1}V_{in} = V_{dc} \tag{5}$$

Similarly, we can generate U_1 to U_{nm} voltages for different switching states.

$$U_1 = V_{11} = V_{21} = \cdots = V_{dc} \tag{6}$$

$$U_2 = V_{11} + V_{21} = V_{i1} + V_{j1} = 2V_{dc} \tag{7}$$

$$U_3 = V_{11} + V_{21} + V_{31} = V_{12} = 3V_{dc} \tag{8}$$

…

$$U_{nm} = m(V_1 + V_2 + \cdots + V_n) = mV_{dc}\sum_{k=1}^{n} 3^{k-1} \tag{9}$$

In the above formulates, i and j are number between 1 to m, the number of the modules. According to the above relationships, the voltage source V_{i1} in any of the modules can be used to generate voltage U_1. There are m choices for generating U_1. For the second level U_2, two V_{i1} sources of two modules must be used. And for voltage U_3, three V_{i1} sources from three modules or one V_{i2} source from one of the modules should be used in series with other circuit equipment. Similarly, for each level, the combination of voltage sources in series can generate the desired level. Finally, to generate the U_{nm} (highest voltage level), all sources (m×n number) must enter the circuit. An essential feature of this configuration with asymmetrical sources and identical modules is the possibility of fault-tolerant, which can be operated with fewer levels if one or more switches or one module are broken due to their parallel diodes.

III. SIMULATION *RESULT*

A. Simulation of 79- Level Inverter

In this section, the simulation of the proposed configuration with asymmetrical sources is investigated. The configuration is composed of three modules, each with three independent DC voltage sources, three switches, and three diodes. As shown in Fig.3, the structure has 13 switches, 9 independent DC voltage sources, and 9 diodes. As mentioned earlier, we have several modes for generating some voltage levels. This converter generates 38 positive voltage levels. The H-bridge is switched at 50Hz frequency and also produces negative and positive voltage levels and zero in the output. So, we have a 79-level output voltage. The upper and the lower switches in the same H bridge leg operate in a complementary manner, so for the H-bridge inverter, we only need two separate gate driver circuits.

$$9V_1 = 9V_4 = 9V_7 = 3V_2 = 3V_5 = 3V_8 = V_3 = V_6 = V_9 = 9V_{dc}$$

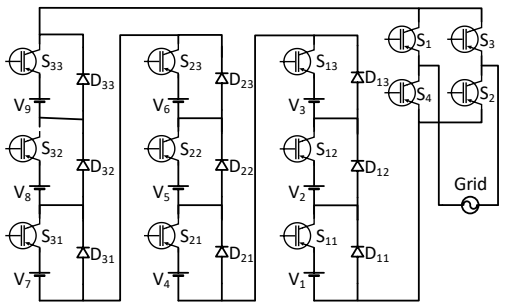
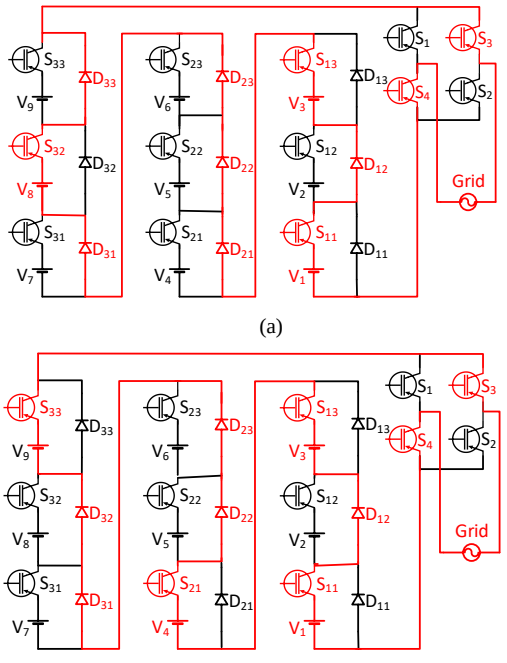


Fig. 3. Configuration of 79 Level Inverter

TABLE I. SWITCHING STATES OF PROPOSED 79-LEVEL INVERTER

No.	S_{33}	S_{32}	S_{31}	S_{23}	S_{22}	S_{21}	S_{13}	S_{12}	S_{11}	V_O
1	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	1	V_{dc}
3	0	0	0	0	0	0	0	1	0	$3V_{dc}$
4	0	0	0	0	0	0	0	1	1	$4V_{dc}$
…	…	…	…	…	…	…	…	…	…	…
134	0	1	0	0	0	0	1	0	1	$13V_{dc}$
135	0	1	0	0	0	0	1	1	0	$15V_{dc}$
136	0	1	0	0	0	0	1	1	1	$16V_{dc}$
…	…	…	…	…	…	…	…	…	…	…
270	1	0	0	0	0	1	1	0	1	$20V_{dc}$
…	…	…	…	…	…	…	…	…	…	…
512	1	1	1	1	1	1	1	1	1	$39V_{dc}$



(a)

(b)

Fig. 4. Two states of switching according to table1 (a) State 134 (b) State 270

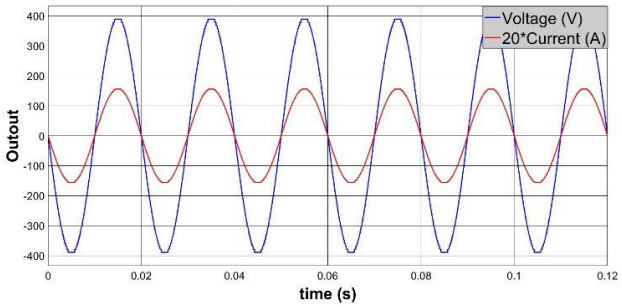
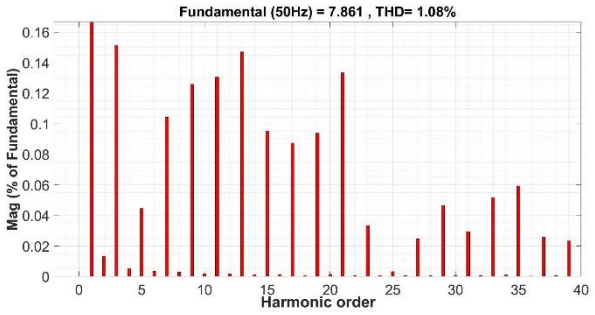
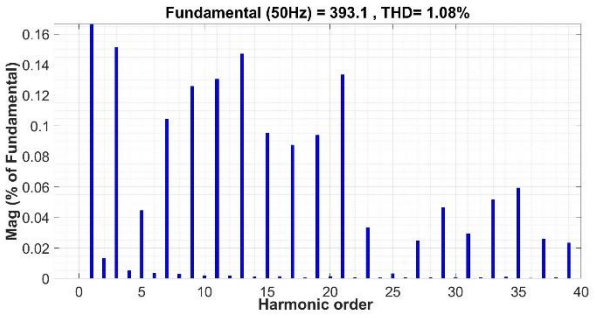


Fig. 5. Output Voltage and Current of proposed 79-Level Inverter



(a)



(b)

Fig. 6. Harmonic order of 79-levels Inverter; (a) Current (b) Voltage

To evaluate the performance of the proposed configuration, the proposed 79-level structure is implemented in MATLAB/ SIMULINK with a 50-ohm resistor as load.

The output voltage and current of the 79-levels inverter are shown in Fig. 5. The THD of voltage and current is shown in Fig. 6.

The PV system output should have low current-distortion levels to ensure that no adverse effects on the other equipment connected to the utility system. To connect the inverter to the grid according to the standard IEC 61727-2004, it is necessary that the output current THD be less than 5%. The maximum allowed harmonics with the order from 2 to 33 are shown in Table. 3. Harmonics of the proposed MLI output voltage and current with pure resistive load is shown in Fig. 6. According to the harmonics shown in Fig. 6, all inverter's current harmonics are less than 0.15%, so no filters are needed. This way, the volume and weight of the converter will be very low.

Table. II. CURRENT DISTORTION LIMIT ACCORDING TO IEC 61727-2004

	Harmonics	Distortion Limit
Odd	3^{rd} through 9^{th}	Less than 4.0 %
	11^{th} through 15^{th}	Less than 2.0 %
	17^{th} through 21^{st}	Less than 1.5 %
	23^{rd} through 33^{rd}	Less than 0.6 %
Even	2rd through 8^{th}	Less than 1.0 %
	10^{th} through 32^{nd}	Less than 0.5 %

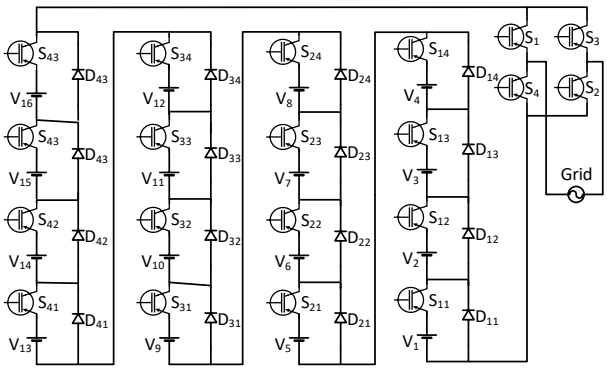


Fig. 7. Configuration of proposed 321-Level Inverter

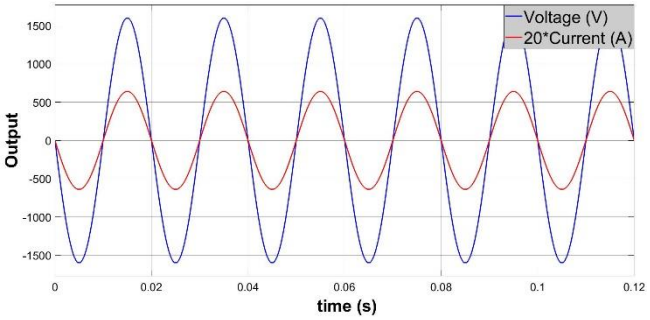


Fig. 8. Output Voltage and Current of proposed 321-Level Inverter

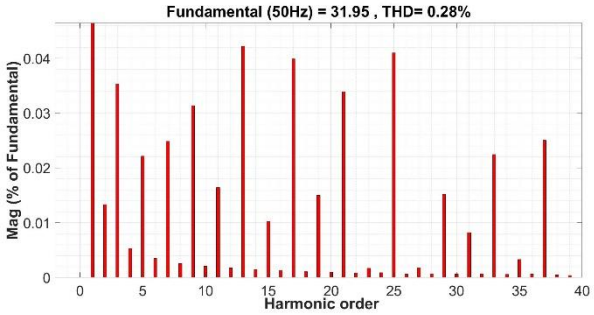


Fig. 9. Harmonic order of 321-levels Inverter Current and Voltage

B. Simulation of 321-Level Inverter

The simulation results for the 321-level inverter are shown in Fig. 7. The voltage and current harmonics of the 321-level inverter's output are shown in Fig. 8. THD of the output current of the proposed MLI is 0.28%, Fig. 9. Again, like a 79-level structure, we don't need extra equipment for filtering to connect to the network.

IV. COMPARISON WITH RECENT TOPOLOGIES

The proposed MLI has two modes of the symmetric and asymmetrical structure. According to Fig. 10, which the number of switches required versus the number of output levels is shown for symmetric-CHB, DC-MLI, FC-MLI, topologies proposed in [14] and [15] and proposed symmetric MLI, the proposed symmetric MLI has a fewer number of switches. In addition, according to Fig. 11, which the number of switches required versus the number of output levels is shown for asymmetrical-CHB and asymmetrical proposed MLI, asymmetrical proposed MLI has the fewest number of switches.

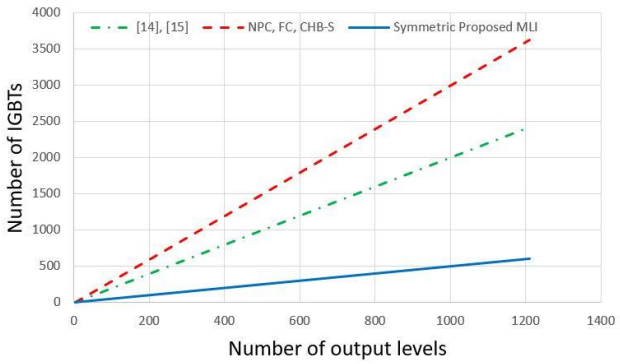


Fig. 10. Comparison between symmetric-CHB, FC, DC MLIs, and proposed topologies in [14] and [15].

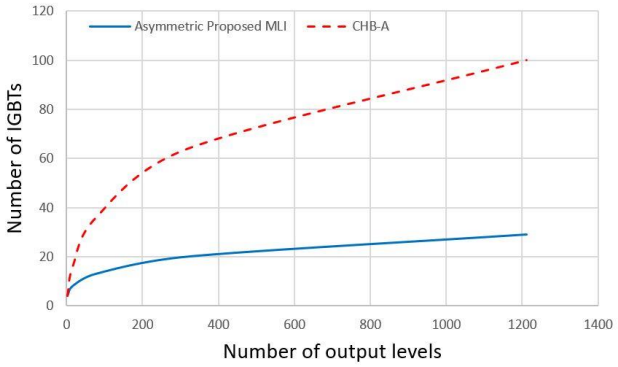


Fig. 11. Comparison between asymmetrical-CHB a proposed MLI

V. CONCLUSION

This paper presents a new configuration of MLIs. The proposed MLI configuration has a much lower number of switches than conventional MLI configuration, with no additional equipment such as inductors and capacitors. This structure is very convenient because of its asymmetrical sources in PV. Also, due to its modular and fault-tolerant structure, if one switch of a module is failed, the switch is bypassed by its parallel diode, and, thus the module can operate properly with a reduced capacity. This structure, with a more significant number of sources, gives much higher voltage levels so that the output voltage becomes almost sinusoidal. For example, this structure, with 25 asymmetrical independent DC sources and only 29 switches, gives 1211 voltage levels. Whereas in asymmetrical CHB mode, we achieve 1211 voltage levels with 25 asymmetrical independent DC sources and 100 switches. So in this structure, there is no need for any filter, and the weight and volume of the converter will be very low.

REFERENCES

[1] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, and series-connected H-bridge multilevel converters," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1032–1040, 2007.

[2] M. Saeedian, M. E. Adabi, S. M. Hosseini, J. Adabi, and E. Pouresmaeil, "A Novel Step-Up Single Source Multilevel Inverter: Topology, Operating Principle, and Modulation," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3269–3282, 2019.

[3] J. N. BhanuTej, C. Rani, A. TamilMaran, J. Santhosh, Y. Wang, and K. Busawon, "Different Multilevel Inverter Topologies and Control Schemes for Renewable Energy Conversions: A Review," *2018 Internat2018 Int. Conf. Comput. Power, Energy, Inf. Commun. (ICCPEIC)ional Conf. Comput. power, energy, Inf.*

Commun., pp. 286–295, 2018.

[4] P. P. Rajeevan, K. Sivakumar, K. Gopakumar, C. Patel, and H. Abu-Rub, "A nine-level inverter topology for medium-voltage induction motor drive with open-end stator winding," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3627–3636, 2013.

[5] P. Samuel, R. Gupta, and D. Chandra, "Grid interface of wind power with large split-winding alternator using cascaded multilevel inverter," *IEEE Trans. Energy Convers.*, vol. 26, no. 1, pp. 299–309, 2011.

[6] J. Rodríguez, S. Member, J. Lai, and S. Member, "Multilevel Inverters : A Survey of Topologies , Controls , and Applications," vol. 49, no. 4, pp. 724–738, 2002.

[7] B. Eskandari, M. T. Bina, and M. A. Golkar, "New concept on sinusoidal modulation for three-phase DC/AC Converters: Analysis and experiments," *IET Power Electron.*, vol. 7, no. 2, pp. 357–365, 2014.

[8] Q. Djudzdo, J. Frp, and S. Jpdlo, "A New 21- Level Asymmetrical Multilevel Inverter Topology with Different PWM Techniques," vol. 3, pp. 1–6.

[9] H. Abu-Rub, A. Iqbal, and J. Guzinski, *High Performance Control of AC Drives with MATLAB/Simulink Models*. Chichester, UK: John Wiley & Sons, Ltd, 2012.

[10] H. A. M. M. K. Al-Haddad, *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*. Chichester, UK: John Wiley & Sons, Ltd, 2014.

[11] A. Delavari, I. Kamwa, and A. Zabihinejad, "A comparative study of different multilevel converter topologies for high power photovoltaic applications," *7th Power Electron. Drive Syst. Technol. Conf. PEDSTC 2016*, no. Pedstc, pp. 415–420, 2016.

[12] N. A. Rahim and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111–2123, 2010.

[13] E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches," *Energy Convers. Manag.*, vol. 50, no. 11, pp. 2761–2767, 2009.

[14] E. Babaei and S. S. Gowgani, "Hybrid multilevel inverter using switched capacitor units," *IEEE Trans. Ind. Electron.*, vol. 61, no. 9, pp. 4614–4621, 2014.

[15] R. Shalchi Alishah, D. Nazarpour, S. H. Hosseini, and M. Sabahi, "Reduction of power electronic elements in multilevel converters using a new cascade structure," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 256–259, 2015.